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Electrochemical fabrication of semiconductor nanostructure arrays for photonic applications

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by

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ABSTRACT

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Theoretical and experimental investigations of the properties of semiconductor nanostructures have been an active area of research due to the enhanced performance that is observed when electrons and holes are spatially confined in one, two or three dimensions. However, the development of viable photonic devices using this phenomenon requires the development of appropriate fabrication techniques that can provide control over nanostructure size, material composition, and periodicity for structures with dimensions less than 20 nm. To address these challenges, a nanostructure synthesis technique has been developed that is based on the self-organization of nanometer scale pores during the anodization of aluminum thin films. This template can then be used for direct synthesis of semiconductor material, or as a pattern transfer mask for the etching of structures in a semiconductor substrate.

In this work, alumina template technology has been transferred from the exclusive use of an aluminum substrate to a thin film technology that can be applied to an arbitrary substrate material. This thin film process has been developed and characterized to permit control and uniformity over both nanostructure length and diameter. In addition, a Al/Pt/Si structure has been developed to permit direct DC synthesis of semiconductor nanostructures. Finally, the ability of this template to serve as a mask for direct etching of nanoscale features on a semiconductor substrate has been evaluated. This technology is currently being developed to provide device applications in the area of photovoltaic devices and silicon electro-optic modulators.

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Chapter 1

Introduction

The development of nanoscale semiconductor devices has been the focus of increasing scientific research during the past 25 years. This high degree of interest is due to the strong enhancement of electronic and optical properties that occurs when electrons are strongly confined in one, two or three dimensions [1]. This research effort has demonstrated that no single fabrication technique is universally applicable for the production of nanometer scale semiconductor devices. Electron-beam lithography [2-4], atomic beam holography [5], and scanning probe lithography [6] are considered to be the preferred methods for the fabrication of low dimensional *electronic* devices [7, 8]. However, for low dimensional *photonic* devices, the use of "nanogrowth" techniques is being investigated to complement the more traditional fabrication methods. These nanogrowth techniques capitalize on the self-patterning of natural systems where the semiconductor material is synthesized in the size and shape of the desired nanostructure. These methods include fabrication of nanostructure arrays using self-organized epitaxial growth [9-14], chemical synthesis of colloidal nanostructures [15-20], synthesis of nanostructures in glass and polymer materials [21-26], and template based chemical synthesis of nanostructures [27-32].

In the specific area of nanoscale optoelectronics, one of the priorities identified by the National Nanostructure Initiative is to develop "new approaches to synthesis and processing that will lead to

affordable commercial fabrication [33]". To meet this goal, it is important to closely tailor fabrication techniques to device requirements and to consider commercial fabrication issues at all stages of research and development. With this in mind, an ideal template for photonic applications should provide: (a) good pore size control and periodicity, (b) good structural and mechanical integrity, (c) chemically inert material for a wide variety of deposited active materials, (d) easily manipulated template size parameters, (e) an economical fabrication process and (f) high transparency over a wide range of the optical spectra. This dissertation will focus on the development of a *thin film porous alumina template* based nanostructure synthesis technique that has the potential to meet the requirements listed above.

1.1 Competing Nanostructure Fabrication Technologies

As mentioned previously, numerous techniques for the fabrication of nanometer scale structures have been developed. Each of these techniques provides a unique strength for a particular application area. In this section, the most popular current techniques will be reviewed and their strengths and weaknesses highlighted.

Porous Silicon

The closest competing technology, and the inspiration for the alumina template technique, is the electrochemical anodization of silicon to form porous silicon. Porous silicon (PS) has been the subject of continuous theoretical and experimental investigations since the first observation of room temperature visible photoluminescence from this material in 1990[34]. Much of this investigation has centered on determining the exact mechanism of light emission in PS, with quantum size effect and emission from Siloxene considered to be the most likely candidates [35]. Recent observations

of continuous tuning of the photoluminescence (PL) spectra with porous silicon nanostructure size [36], the correlation between PL blue shift and radiative lifetime [37], and the observation of transverse-optical (TO) photon replicas in resonantly-excited PL spectra [38] indicate that the quantum size effect is at least partly responsible for producing the observed luminescence in porous silicon. These results are supplemented by the observation of a shift in the PL and absorption spectrum of porous silicon with an applied electric field consistent with the Quantum Confined Stark Effect (QCSE). This result is discussed in more detail in Appendix A [39].

Porous silicon is fabricated by the electrochemical anodic etching of crystalline silicon in an HF solution. The resulting material structure has best been described as an interconnected network of nanoscale silicon structures with varying size and dimensionality [40]. As a result of this size variation, porous silicon shows a broad emission band as a function of wavelength (on the order of 300nm). The lack of a narrow emission linewidth, coupled with the delicate physical nature of the porous silicon structures has limited device applications using this material. Phillip Fauchet at the University of Rochester has demonstrated the integration of room temperature LEDs with silicon bipolar junction transistor devices [40]. However, the lifetime of the optically active structures is not reported. The primary degradation mechanism for porous silicon is an "aging effect" related to oxidation of the silicon nanostructures [40]. Due to the size (~ 2 nm) and large surface are of the nanostructures, native oxide formation can significantly degrade device performance by causing a relatively large change in material diameter. Perhaps the most promising application for porous silicon is its use as an integrated visible and infrared optical waveguide material with reported losses down to 1 dB/cm [41, 42], or as an anti-reflection coating for crystalline silicon photovoltaic cells.

In summary, the porous silicon fabrication technique provides the ability to form highly luminescent structures using an indirect band-gap substrate (silicon). A primary limitation of this approach has

been the inability to identify an appropriate encapsulation material for the porous silicon. As a result, mechanical damage to the nanostructures and chemical aging effects significantly reduce the reliability and operational lifetime of fabricated devices. This technique is compatible with conventional silicon CMOS processing, primarily due to the ability to use conventional photoresists to mask the HF etching process.

Lithographic Techniques

The traditional and most precise method for nanostructure formation is the use of lithographic techniques coupled with MBE/MOCVD material growth. While electron beam lithogaphy remains the standard nano-pattern definition technique, scanning probe microscopy (SPM) and atomic beam hologaphy have begun to be used for nanoscale device fabrication [3, 43, 44].

The minimum feature size for electron-beam lithography is primarily limited by the resist material used, with a feature size of 7 nm reported using a methylstyrene resist [7]. While this feature size is small in comparison to most devices, it is important to remember that porous silicon is composed of a large number of structures with sizes down to 2 nm, and pores in alumina have been demonstrated down to 4 nm. Therefore, while electron-beam lithography can provide precise placement and definition of small structures, the minimum feature size is still larger than that obtained with other non-lithographic techniques. The second limitation of e-beam lithography is the serial nature of the approach and the Coloumb interaction between electrons in the beam. While a number of attempts to relax these limitations have been proposed [3], none have been able to demonstrate a throughput close to that needed to form dense arrays of individual nanostructures. A final concern with e-beam lithography is defect creation in the semiconductor material from the energy transfer of the electron beam to the substrate material [45]. For the case of semiconductor

nanostructrues, this damage can result in pinning of the Fermi level at the surface, resulting in a variation in the effective electrical size of the nanostructure.

An interesting technique to relax these limitations is the use of atomic beam holography [46, 47]. In this approach, atoms (typically Ne) are cooled to ultra-low temperature (50 μK) and diffracted through a computer generated hologram [7]. The potential advantages of this approach are that it can provide nanometer scale lithographic definition (~ 5 nm) over a large area (~10 microns) without the use of energetic particles. While this technique is promising, there are several significant limiations. The first is that the minimum feature size actually obtained at present is on the millimeter scale. In addition, this feature size was obtained using a micro-channel plate (MCP) and not with a resist material. As seen with e-beam lithography, the primary limiting factor in obtaining an ultimate minimum size may be the development of an appropriate resist than can provide both feature resolution as well as appropriate resistance to various etch techniques. Finally, the expense of the atomic beam generation and cooling systems (as well as holographic mask fabrication) may limit initial development of this approach. However, the initial capital cost may not be an issue for commercial integrated circuit processing assuming that a sufficient wafer throughput can be maintained.

The most precise method for fabricating nanometer scale structures is the use of scanning probe lithography [6, 44, 48, 49]. Using this technique, semiconductor structures can be patterned by: (a) low energy exposure of resists, (b) thermo-mechanical writing, (c) local oxidation, (d) mechanical modification, and (e) nanomanipulation [6]. The primary limitation of this approach is the extremely low throughput of feature definition. In addition, the definition of nanometer scale features requires the use of an ultra-high vacuum system and substantial vibration isolation equipment. One possible method to improve throughput with this approach is to use a "massively-parallel" arrays of probe

tips. However, no effective method of addressing and controlling such an array of probes has been presented at this time.

In summary, lithographic techniques currently appear to be the most effective method for the fabrication of nanoscale *electronic* devices. This is due to the requirement to produce nanometer-scale structures where device functionality is the result of the interconnection between individual structures. There are no fundamental limitations on size, shape, or composition of the nanostructurses, or on the active materials. The primary limiting factor of these techniques is not necessarily performance, but the ability to generate a low enough cost-of-ownership to enable commercial operation.

Heteroepitaxial Self Assembled Structures

The primary technique used for the development of quantum dot lasers is the self-assembly of quantum dots during MBE/MOVPE heteroepitaxy [13, 50-60]. This approach relies on non-equilibrium heteroepitaxial growth utilizing a stepped (vicinal) surface as a template [61]. The primary advantage of this approach is the excellent material quality resulting from the MBE/MOVPE growth and the lack of an etching/lithography step that can result in material damage. By varying the growth properties the structures can range from quantum wires to "strings of quantum dots" [61]. While lasing has been demonstrated due to the high material quality, and low threshold has been observed due to the low discrete density of states in quantum dots, these structures tend to have significant inhomogeneous line broadening due to variation in nanostructure size [50].

This approach can provide structures ranging from quantum dots to quantum wires by varying the material deposition properties. The composition of the nanostructures is limited to III-V and II-VI

elements that can be deposited by MOVPE or MBE techniques. In addition, the use of a given substrate material limits the choice of deposited nanostructure material to maintain quantum confinement. As presently constructed, this technique is not compatible with silicon CMOS processing due to the requirement for a stepped (vicinal) substrate to prevent anti-phase disorder (APD) [62].

Colloidal Semiconductors

The preparation of colloidal semiconductors in solution provides the best method for experimental verification of theoretical results in the physics of nanostructures. Using colloidal techniques, solutions with nearly monodisperse particle size distributions with uniform spherical shape and sizes down to 1.5 nm can be formed [63]. In addition, by coating the particles with an appropriate organic shell [64], electrons or holes can be rapidly removed from the quantum dot, allowing observation of carrier relaxation dynamics by infrared pump-probe spectroscopy. Using this technique, the "phonon bottleneck" in quantum dots was observed for the first time experimentally [65].

Using this technique a number of III-V, IV, and II-VI semiconductor quantum dots have been synthesized in solution. The size distribution is highly uniform and the nanostructures are generally spherical. The primary limitation of this approach is that the colloids are synthesized in solution, and as a result using these structures for device applications has been problematic. Deposition and drying of the solution on a substrate material results in clumping of the individual particles with loss of quantum confinement [15].

Doped Glasses

One of the oldest methods of semiconductor nanocrystal synthesis has been the heat treatment of a glass host doped with semiconductor precursors (e.g. CdO and Te). After heat treatment homogeneous nucleation of the semiconductor precursors results in the formation of nanocrystals within the transparent host material [21, 22, 66, 67]. Using this approach , nanostructures with good size distribution (~6 %) and small size (~ 3 nm) can be formed. The primary limitation of this approach is the high process temperature required to melt the glass host material, and the lack of control over nanocrystal periodicity.

The advantages of this approach is that it provides quantum dot formation at relatively low cost with excellent encapsulation. However, this encapsulation also limits the ability to contact the nanostructures for detector applications. CMOS applications are limited due to the requirement to deposit the material as a molten glass.

Template Based Approaches

In addition to the use of an anodized aluminum template, several other template based approaches have been reported. One of the earliest reported non-lithographic nanostructure fabrication techniques is based on the use of track-etched polymer membranes. In this approach, nanometer scale damage paths are formed in a polymer material as the result of irradiation by heavy ions. The resulting damage paths can be etched resulting in pores with diameters down to 30 nm and lengths of up to several microns. Active superconductor and metals can then be deposited in the pores using standard chemical synthesis techniques. The primary application area for this approach has been in the investigation of giant-magnetoresistance effects in metal nanowires [68-70]. The limitations of polymer track membranes are relatively large pore diameters (30 nm), lack of size control, and lack of pore periodicity.

A second approach is the use of zeolite structures as a template for chemical synthesis of semiconductor nanostructures. In particular, the MCM-41 host material has been used to synthesize a number of semiconductor materials including CdSe [32], Si [71], Ge [72], InP [73], GaAs [73], CdS [74], and GaN [75, 76]. MCM-41 provides a hexagonal array of cylindrical pores with diameters down to 2.7 nm and a reported size distribution (FWHM of 0.2 nm) calculated by N_2 desorption data [32]. However, there is no evidence that this technique has been used to form thin films of nanostructures. Instead, the zeolite host material is used in powder form, washed with toluene to remove excess material, and precipitated as a powder with MCM-41 loaded semiconductor nanostructures [32]. According to the various reports, this is done to allow characterization by various analytical techniques. However, it is significant to note that no reference is made to optical characterization of the thin film nanostructure arrays.

The final template based synthesis method to be discussed is the use of carbon nanotubes. Carbon nanotubes have been synthesized in alumina templates to from fixed parallel arrays of nanotubes [77-79]. In addition, there is one report of using a carbon nanotube as a template for chemical synthesis of semiconductor material [80]. However, this tends to be a "template within a template approach" and does not appear to provide significant fabrication or application advantages.

Summary

A number of semiconductor nanostructure fabrication techniques have been demonstrated that have potential for very specific applications. In particular, the use of lithographic techniques provides the greatest control over size and shape for research applications. However, the development of sufficient throughput for volume production remains the fundamental challenge. Porous silicon remains a popular technique due to its ability to directly provide luminescent structures using a silicon substrate. However, unless the particle size distribution and encapsulation issues are

addressed, this technique does not appear to have significant device applications. Heteroepitaxial techniques are primarily restricted to the development of quantum dot lasers. This approach provides the highest level of material quality, however, size distribution and uniformity are not significantly improved over other less expensive techniques. Doped glasses have been used to demonstrate high performance optical modulators [81] and provide excellent encapsulation of the nanostructures. However, integration issues and poor nanostructure periodicity limit this approach.

1.2 Alumina Template Approach

The primary focus of this dissertation is the development of a non-lithographic fabrication technique based on the electrochemical synthesis of compound semiconductor material using a template ofanodized alumina. A basic overview of this technique is presented in this section and is discussed in more detail in Chapters 2 and 3.

When aluminum is anodized in an appropriate acidic electrolyte under controlled conditions, it oxidizes to form a hydrated aluminum oxide (alumina) containing a two dimensional hexagonal array of cylindrical pores as schematically shown in Figure 1-1. The pore diameter and the inter-

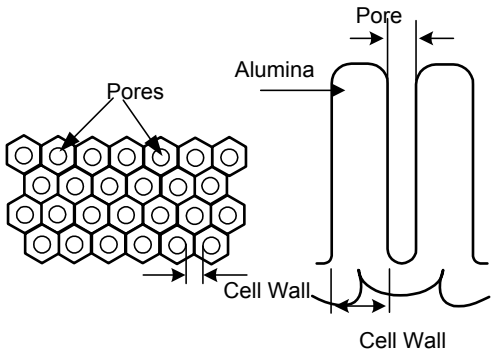

Figure 1-1: Top view and cross-sectional view of a schematic of the alumina pore structure.

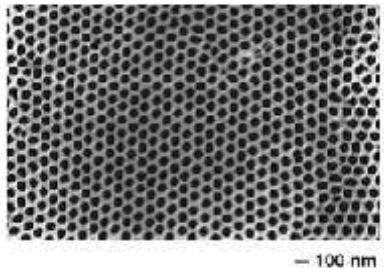

Figure 1-2: FESEM image of highly ordered pores on bulk aluminum.

pore spacing depend on the anodization conditions such as electrolyte pH, temperature, anodization current density, and aluminum microstructure (grain size). Pores can be up to several microns in depth. The anodization parameters can be precisely controlled to form pore diameters between 4 and 100 nm with less than 10% variance in the pore size distribution in bulk aluminum (Figure 1-2). As a result anodized alumina can act as ideal templates for the fabrication of periodic semiconductor nanostructure arrays for photonic and electronic applications if similar order can be obtained for thin films. Anodization is performed in a simple wet chemistry apparatus where the aluminum layer is polarized as the anode (positive), and a platinum electrode is used as the cathode (negative).

Anodization can be performed under constant DC current (galvanostatic) or constant DC voltage conditions (potentiostatic). Sulfuric acid and oxalic acid are typically used for the anodization of aluminum. During the first 3-5 seconds of anodization, a thin continuous film of alumina, called the barrier layer, is formed on top of the aluminum substrate. As anodization is continued, an array of pores begins to develop in the barrier layer. The pore diameters increase until reaching a steady state dimension determined by the anodization conditions. When the steady-state diameter is reached, the pores grow in depth at a rate proportional to the anodization current density until the aluminum has been exhausted or until the applied current is removed. Therefore both the pore diameter, which is solely determined by the anodization conditions, and the pore depth, which can be determined from the linear pore formation rate, can be precisely controlled. This allows the properties of the nanostructure to be varied between those of a quasi-spherical quantum dot (confinement in three dimensions) to a quantum wire (confinement in two dimensions). The evolution of the optical and electrical properties of these structures as a function of the confinement dimension has been recently been shown by Susa [82].

The active semiconductor material for the nanostructures is formed by electrochemical synthesis or colloidal deposition inside the pores. The in-situ electrochemical synthesis of active materials within the pores has been well investigated by our group as well as a number of other researchers [83, 84]. Some of the species introduced into the bulk nanoporous alumina are: gold, nickel, iron, CdS, CdTe, ZnS, CdSe, GaAs and ternary semiconductor compounds ($Cd_xZn_{1-x}S$). In particular, Cadium Sulfide has been a well-investigated system both by our group and other researchers due to its high degree of optical activity and non-linear optical properties. In addition, the synthesis of narrow band-gap (e.g. InAs) semiconductors through the electrophoretic deposition of colloidal materials is currently being investigated in collaboration with the University of Notre Dame.

1.3 Problem Statement

The formation of semiconductor and metallic nanostructures using alumina templates formed on bulk aluminum substrates has been demonstrated by a number of researchers [77, 78, 80, 85-97]. However the use of an aluminum substrate is problematic for two primary reasons. First, it is difficult to obtain aluminum substrates with a high level of material purity and a low degree of surface roughness. Second, it is difficult to integrate the devices produced with other electronic or photonic components such as transistors or waveguides. Therefore, it is desirable to be able to create templates with high uniformity using an aluminum thin film deposited on an arbitrary substrate material. After templates have been created with a high degree of periodicity and size control, the next concern is the ability to use this to create semiconductor nanostructures with useful properties for device applications. Finally, once arrays of nanostructures have been created, it is necessary to be able to determine if a viable device applications exists for the material that has been created.

To address the challenges in the previous paragraph, three specific research goals have been identified:

1) To create and characterize thin film alumina templates on multiple substrate materials.

2) To develop a process that enables the synthesis of semiconductor nanostructures with the level of material quality required for photonic applications.

3) To identify commercially viable device applications for this technology.

In summary, the primary objective of this dissertation is to determine if the fabrication of semiconductor nanostructures using a preformed alumina template is viable for photonic device applications. Then, given that this objective is met, to lay the foundation for future research using this technique.

1.4 Dissertation Outline

Chapter two will provide an overview of the anodization of bulk aluminum and the extension of this technique to thin film alumina templates on a variety of substrate materials. In addition, the characterization of these templates by imaging, photoluminescence, and electrical techniques will be discussed.

In chapter three, the electrochemical synthesis of compound semiconductor materials into the alumina template pores will be presented. This will include an overview of quasi-electrochemical techniques, AC nonaqueous deposition, DC nonaqueous deposition, and underpotential deposition.

Chapter four will discuss the use of the alumina template to create a pattern transfer mask for the creation of nanostructure in a silicon substrate. Three different techniques to accomplish this will be presented: porous silicon formation, RIE pattern transfer, and RIE image reversal.

Chapter five will present device applications of this technology in the development of photovoltaic devices. In particular, the use of semiconductor nanostructures synthesized in the template pores for the creation of multijunction solar cells will be discussed. In addition, the use of this technique to create subwavelength textured surfaces will be analyzed.

In chapters six and seven the conclusions that can be drawn from this research as well as future work will be presented.

Finally, Appendix A and B will contain previous work in the area of porous silicon not directly related to the major topic of this dissertation.

Chapter 2

Alumina Template Fabrication and Characterization

When aluminum is anodized in an oxidizing electrolyte, a thin layer of hydrated aluminum oxide, or alumina is formed. Depending on the strength of the acidic solution used, field enhanced oxide dissolution can compete with the aluminum oxidation process to from a material with nanometer-scale pores. This property has been used since the 1930's to provide both corrosion protection for aluminum parts as well as to dye these materials. However, during the 1990's it was realized that the pores in alumina could provide a template for the synthesis of both semiconductor and metal nanostructures . In fact the alumina material provides an almost ideal template since it can provide periodic pores with good control over the size distribution, is transparent over the visible spectrum, is electrically insulating, and is relatively corrosion resistant [98]. The primary limitation to the development of photonic devices using this approach has been the requirement to use an aluminum substrate. The objective of this dissertation research has been to by investigating the formation of an ordered porous alumina thin film on an arbitrary substrate material.

In this chapter, alumina formation on bulk substrates will be discussed along with recent work describing the formation of self-ordered structures. Then the extension of this work to semiconductor substrates will be presented. Finally the characterization of these templates using imaging, optical and electrical techniques will be discussed.

2.1 Bulk Alumina Formation

Initial formation of alumina can be the result of a spontaneous reaction between aluminum and oxygen than results in the creation of an insoluble anhydrous aluminum oxide layer. The self-limited formation of this nanometer scale layer can then protect the remaining aluminum from further chemical reaction. Since this is a spontaneous chemical process, it cannot be easily controlled and is assumed to always exist on an aluminum surface. It is for this reason that in aluminum RIE etch procedures, an aluminum oxide etch is conducted before the aluminum etch.

When aluminum is immersed in an electrolyte and a potential is applied, the formation of thicker oxides can take place. In the case of anodization in neutral (pH 7-8) solutions, a non-porous oxide is formed. The thickness of this oxide is limited to several hundred nanometers, after which dielectric breakdown of the oxide creates a short circuit ending the electrochemical reaction [99]. For the case of strong acids (sulfuric, phosphoric, oxalic) field assisted oxide dissolution results in the formation of a close-packed array of columnar hexagonal cells. Due to the porous structure of the films, charge transport takes place only across the barrier layer removing dielectric breakdown as a thickness limiting mechanism.

Keller, Hunter, and Robinson first characterized porous alumina as a close-packed array of columnar hexagonal cells each containing a central pore normal to the substrate surface [100]. A schematic of the Keller model is shown in Figure 2-1. While several other models to explain certain aspects of pore formation have also been developed, for this work the Keller model remains the most relevant.

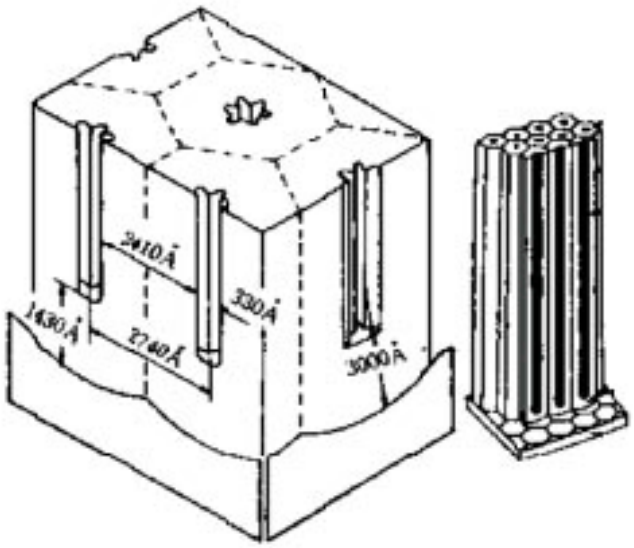

Figure 2-1: Schematic of the Keller model for pore formation in anodic alumina.

The electrochemical anodization of aluminum to form alumina takes place in several discrete steps. During the first 3-5 seconds of anodization, a thin non-porous film of alumina (Al_2O_3) called the barrier layer, is formed on the aluminum surface. As anodization proceeds, an array of pores develops on the barrier layer, whose diameters increase until reaching a final dimension determined by the anodization conditions. Once the final diameter is reached, the diameter of the pores do not increase any further, and as the anodization is continued, the pore depths increase at a rate proportional to the anodization current. A convenient way to monitor the anodization process is to observe the voltage-time characteristics measured between the anode and the cathode. Since the potential across the device is proportional to the device resistance, it increases during the first 3-5 seconds when the high resistance barrier layer is formed. Next, as the pores begin to develop, the

potential decreases until the final pore diameter is reached, after which the potential remains constant as the pores propagate. A schematic of the pore formation process for an alumina thin film on bulk aluminum is shown in Figure 2-2

The initial formation of the barrier layer material is the same for the creation of both porous and non-porous oxides. As the temperature increases, the maximum voltage increases and the position

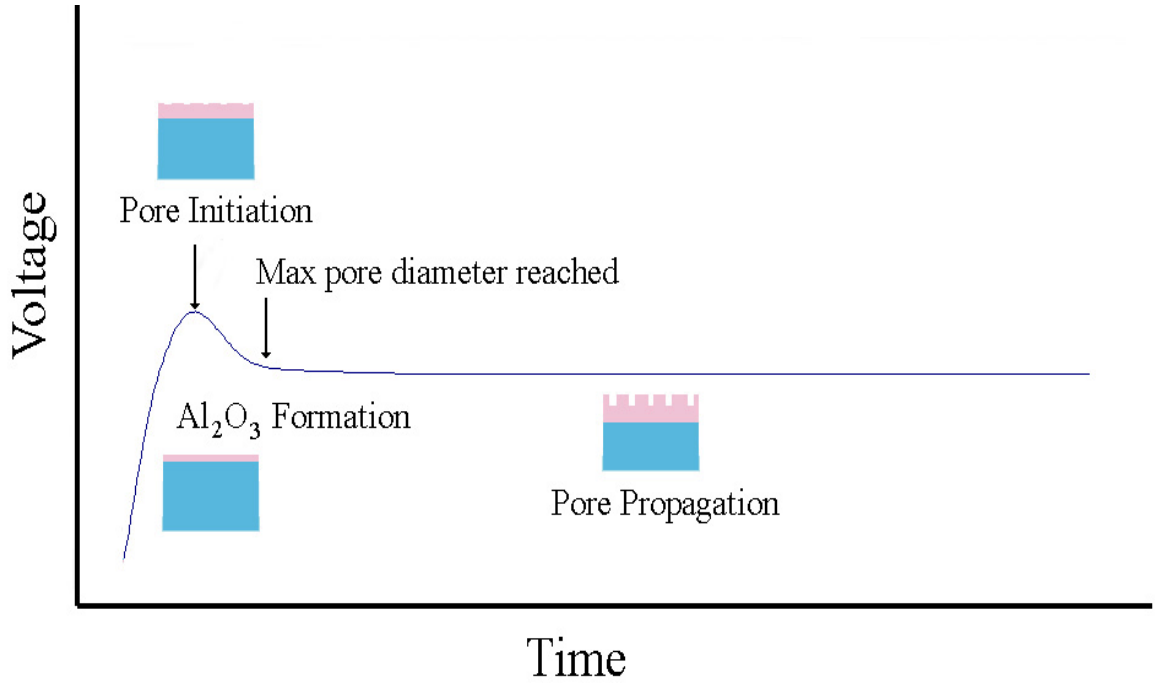

Figure 2-2: Voltage time characteristics during anodization of bulk aluminum

of this maximum occurs earlier in the anodization process. After this maximum potential is reached, pore nucleation begins at the alumina surface and results in a decrease in the potential until a steady state situation is reached. The initial nucleation of pores on the alumina surface is believed to follow initial roughness in the barrier alumina film [99]. Since the electric field around an asperity is enhanced [101], a non-uniform dissolution of alumina at the electrolyte interface is created.

After pores are nucleated, they reach a final fixed diameter and begin to propagate through the growing aluminum oxide (alumina). The exact mechanism for this behavior is not clear. It has been suggested that ohmic control of the surface at the pore mouth, or an automatic adjustment of surface film properties that stabilizes a fixed pore size [101] is responsible for this effect. For the case of alumina formed using a bulk aluminum substrate, the voltage remains constant until anodization is completed, or until the substrate is completely anodized. Since the electrochemical oxidation front proceeds ahead of pore formation, a barrier layer of thickness equal to the pore diameter separates the pore from the non-oxidized aluminum.

2.1.1 Pore Self-Organization

It has been experimentally observed that as the anodization process continues, the initial randomly nucleated pores begin to organize into a hexagonal array and the pore size distribution is reduced [102]. The mechanism for this behavior is currently believed to result from the formation of repulsive forces between pores due to mechanical stress in the alumina film [103]. In [103] it is shown that the configuration for lowest mechanical stress in the alumina film is a hexagonal array of uniform pores.

There appear to be two methods to obtain highly ordered pore structures in alumina thin films. First, since pore nucleation is determined by electric field variation at the alumina/electrolyte interface, the alumina surface can be pre-patterned to obtain uniform pore nucleation. Second, the natural tendency of the porous alumina to relax to its lowest stress state during anodization can be used to create a highly-ordered hexagonal array of pores.

There have been several significant attempts to provide ordered pore nucleation. Masuda has used a silicon carbide "nano-stamp" to create preferential nucleation sites for pore growth [104]. This technique involves the creation of a SiC master mold on which the desired pore pattern has been created by electron-beam lithography. The master mold is then applied to the aluminum surface at very high pressure (5 ton/cm^2). This technique has demonstrated that control of pore nucleation can lead to highly ordered pore structures. However this approach is not viable for device applications since the master stamp is rapidly damaged due to the high pressures used in the pattern transfer process. A second technique is the formation of an ordered structure through electropolishing of aluminum in a perchloric acid solution [105]. This technique has also resulted in the formation of highly ordered pore arrays. Unfortunately, the smallest pore size that can be created with this technique is 50-55 nm due to the electropolishing dynamics. In addition, the high etch rate of electropolishing (~1 micron/sec) makes this technique impractical for thin film applications.

The use of the inherent self-organization in porous alumina films appears to provide a more viable approach for template formation. Very long anodization times (~ days) have demonstrated that as the anodization time approaches infinity, nearly perfect pore order is created [106]. This has been shown even for the case of significant defects in pore nucleation. Using his SiC stamping process, Masuda has recently shown that the alumina templates have the ability to "self-repair" defects in the pore structure after long anodization times [107].

A combination of these two techniques has been developed resulting in a multi-step anodization process [106]. In this approach the aluminum substrate is partially anodized and then the porous alumina is removed in a solution of phosphoric and chromic acid. Due to the presence of chromic acid, there is a high degree of etch selectivity and the remaining aluminum material is not etched. Therefore, the imprint of the pore bottoms remains at the surface of the aluminum substrate. This

is then used as a preferential pore nucleation site for the next anodization cycle. This process can be repeated as many times as necessary given a sufficient aluminum thickness. Since the template is removed, pore organization can proceed at a faster rate and pore order equivalent to the anodization of several millimeters of film can be obtained with a starting material of less than one micron [106].

2.2 Alumina Thin Film Templates

The fabrication of alumina thin films on bulk substrates has demonstrated the feasibility of this approach for nanostructure synthesis. However, for the development of photonic applications, thin film templates with flexibility in the choice of substrate material is desired. In this section, the work to develop the thin film template technology is described. In particular, the methods for thin film deposition, template anodization, and pore widening will be presented. Finally, the development of a platinum/alumina structure will be presented that allows the formation of single crystal semiconductor nanostructures.

Aluminum Thin Film Deposition

The use of magnetron sputter deposition, thermal evaporation, and electron-beam evaporation were investigated for the creation of aluminum thin films for template fabrication. The first technique attempted was thermal evaporation of 99.999% Al pellets in a thermal evaporation system refurbished by the Nanostructures Research Group [108]. This system is pumped with a Varian diffusion pump and is operated at a base pressure of $5x10^{-6}$. The potential-time profile during anodization showed the basic features expected during anodization. However the slow rise in potential during pore propagation is believed to result from non-uniform anodization of the deposited film. In addition, visual inspection of the anodized layer revealed non-uniform adhesion

to the silicon substrate. These effects are believed to result from non-uniform aluminum deposition caused by a problem with the planetary rotation system.

The second method investigated was magnetron sputtering of both 99.999% Al as well as an Al-Cu alloy (99.999% purity.) Sputtering was preformed in a cryo-pumped deposition system in an Argon atmosphere with base pressure of 1.0×10^{-6}. This deposition technique (without substrate heating) resulted in substantial roughness in the deposited aluminum material. An AFM image of the deposited film is shown in Figure 2-3.

The final method used for thin film deposition was electron-beam evaporation of 99.999% Al using a cryo-pumped system at a pressure of 5×10^{-7}. This was accomplished at the University of Notre Dame. This technique appears to provide enhanced uniformity in the deposited layer as well as decreased surface roughness. This technique is currently the primary method of deposition of aluminum thin films in this research except where noted.

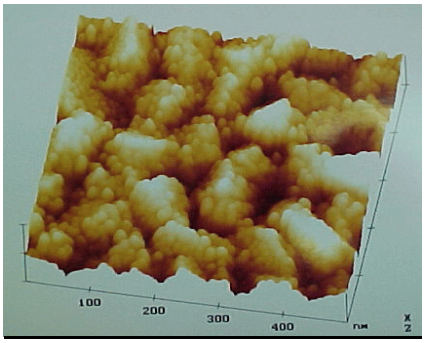

Figure 2-3: AFM Image of deposited aluminum film.

Anodization

Template formation was performed by anodization in a solution of 20% (v/v) H_2SO_4 at a temperature of3°C. The low anodization temperature is used for two reasons. First, Masuda has experimentally demonstrated that low anodization temperature (< 3° C) significantly increases pore uniformity. The second reason is that alumina is weakly soluble in sulfuric acid leading to an undesirable isotropic etching of the alumina pores. This effect can be eliminated by a reduction in the anodization temperature since chemical etching is a thermally activated process. This is similar to the use of a liquid-nitrogen cooled stage during deep-trench silicon RIE to increase etch anisotropy.

A potential time characteristic for anodization on a silicon substrate is shown in Figure 2-4. When compared with anodization on a bulk substrate, the early stages of barrier layer formation, pore nucleation, and pore propagation are not effected. However, a rapid increase in potential is seen as the aluminum oxidation front hits the silicon surface. This feature is unique to anodization on non-aluminum substrates and is strongly dependent on the substrate characteristics (type, doping,

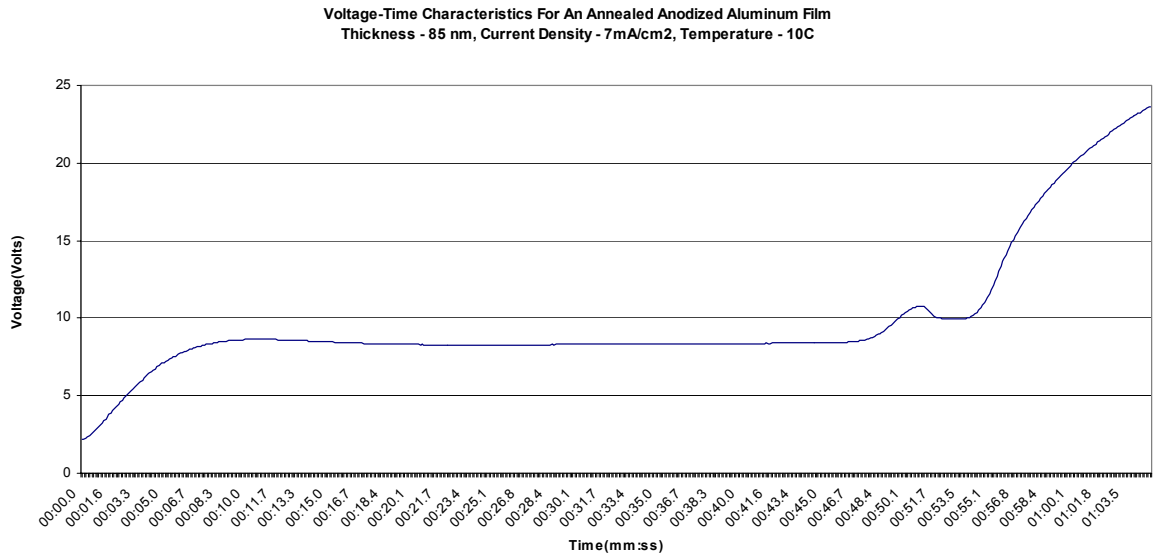

Figure 2-4: Potential time characteristic for template anodization on silicon.

annealing). It is believed that the rapid increase in potential results from the anodic oxidation of the silicon substrate. To verify this theory, an alumina template was formed on a silicon substrate and the anodization current was left on for 15 seconds after the potential reached the maximum allowed by the power supply (30 V). Then, the template was removed by a phosphoric acid etch. Since there is a large degree of etch selectivity between alumina and silicon dioxide (> 100:1), this etch should not have altered any silicon dioxide formed. The substrate was then imaged using a LEO 1530 FESEM at the Penn State National Nanofabrication Users Facility with a representative image shown in Figure 2-5. The detection of a two layer structure and the observation of significant charging strongly suggest that an oxide was formed at the silicon/alumina interface. However, the structural composition and stoichiometry of this oxide have not been determined.

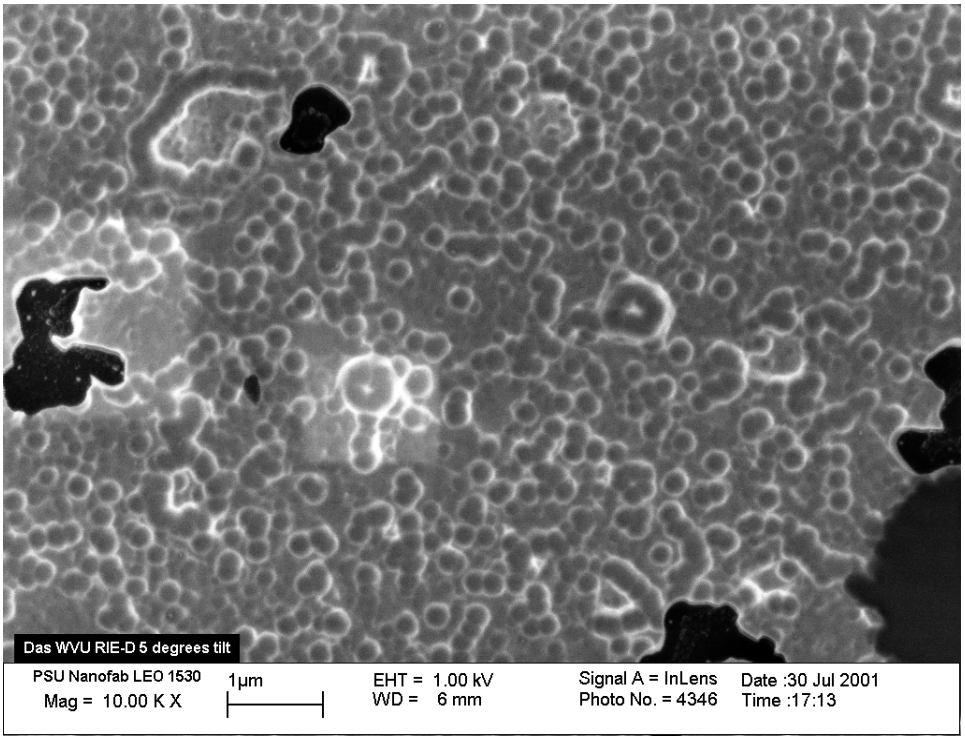

Figure 2-5: FESEM image showing silicon oxide formed during anodization.

A significant advantage of using an alumina template on a silicon substrate is that the anodization rate can be determined by monitoring the time between the initiation of anodization until the rapid rise in potential at the silicon surface is observed. The anodization rate was determined as a function of current density in collaboration with Paul Sines for a variety of anodization temperatures and film thicknesses. These results are shown in Figure 2-6 and indicate a linear dependence between anodization rate and current density, especially at low current densities.

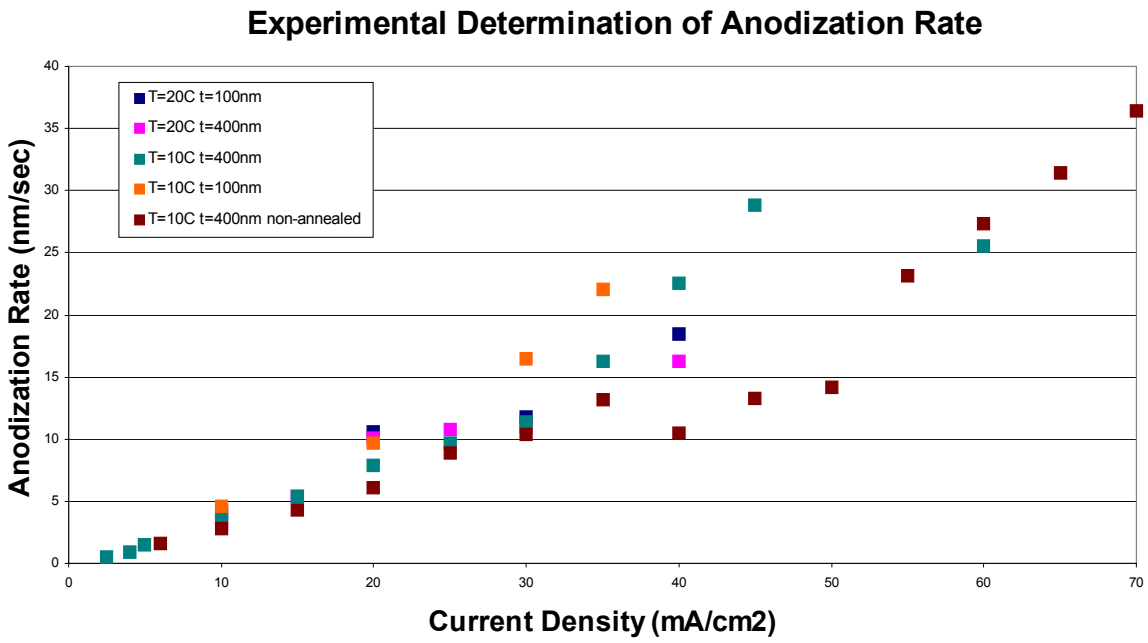

Figure 2-6: Experimental determination of anodization rate as a function of current density.

Pore Widening

Pore widening in 5% phosphoric acid is performed after anodization to remove the top surface of the alumina template where non-uniform pore nucleation has occurred. This technique can also be used to chemically remove the alumina barrier layer as well as to increase the average pore diameter.

One concern during pore widening is to ensure a uniform distribution of the acidic solution within the porous structure to ensure uniform chemical dissolution. To enhance uniform etching, the templates are soaked in de-ionized (DI) water for approximately 12 hours to equilibrate the template and reduce the effect of surface tension at the pore mouths.

Barrier Layer Engineering

A technological limitation to the development of this template based nanostructure technology is the presence of an alumina barrier layer at the bottom of the pore. This can be chemically etched using the pore widening process, however there is a narrow process window between complete barrier layer removal and complete liftoff of the template. In the case of bulk alumina templates, the barrier layer is detached from the substrate by etching in mercury chloride which also serves to eliminate the barrier layer. A second concern is the formation of an oxide layer on the substrate at the alumina/substrate interface. This was shown previously in the case of silicon, however a similar anodic oxidation (or substantial substrate etching) occurs for most other materials [109].

Two approaches were investigated for addressing the barrier layer issue and substrate oxidation. The first approach is to use a conductive oxide (i.e. ITO) as an interfacial layer (i.e., aluminum/ITO/silicon) to prevent oxidation of the silicon surface. Previous work tends to indicate that ITO is stable under electrochemical processing [110]. However, to determine this for the specific processing conditions used in template formation, this was experimentally investigated using ITO coated glass-slides (R_s=4-8 Ω) purchased from Digital Technologies, LTD. An aluminum thin film was deposited by magnetron sputter deposition and was anodized in sulfuric acid. The potential-time profile is shown in Figure 2-7. This result tends to indicate that alumina

was formed on the templates, however the noise during the end of pore propagation suggests the presence of an adverse chemical reaction at the alumina/ITO interface.

At the same time, the use of an aluminum/platinum/silicon structure was investigated. In this case, a 50 nm Pt film was deposited by electron-beam evaporation followed by a 500 nm Al film without breaking vacuum. The template was then anodized using a constant voltage and an unusual effect was observed. Instead of the rapid increase in resistance seen in every other material, the resistance remained constant, although a substantial amount of noise was detected. A top view and cross-sectional view of the fabricated structure is shown in Figure 2-8 and 2-9 respectively.

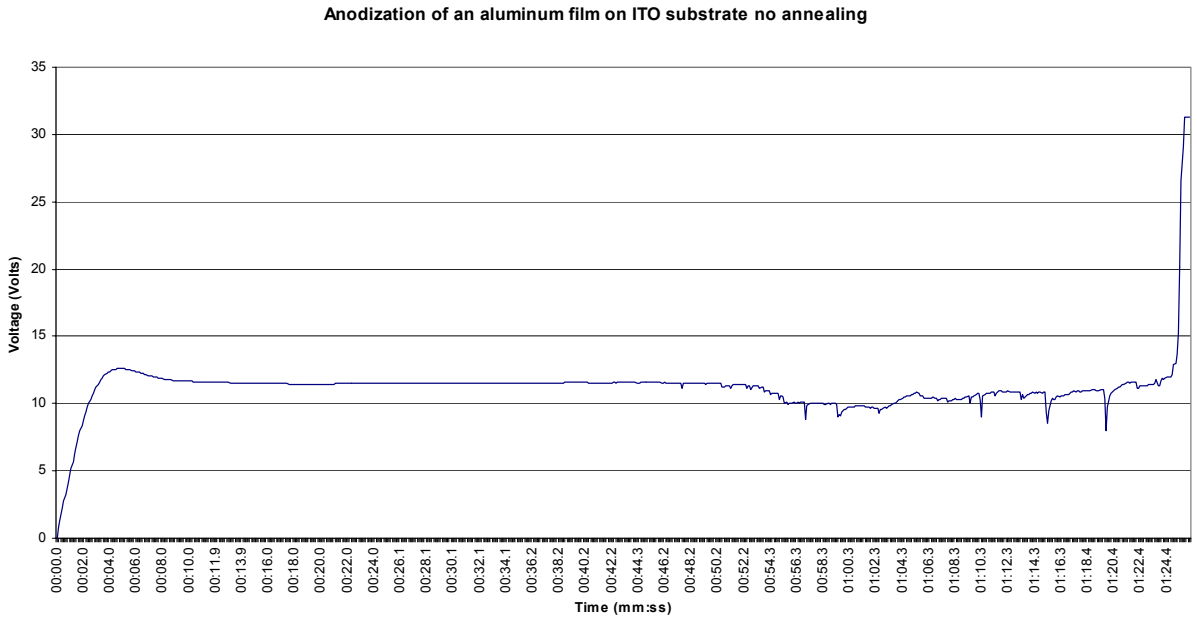

Figure 2-7: Potential time characteristic for the alumina formation on an ITO coated glass substrate.

Figure 2-8 shows that an ordered alumina template was formed for the Al/Pt/Si structure. The cross-sectional image shows that the pores are normal to the Pt layer and that the barrier layer is absent. This is confirmed by noting that the angle between the pore and the Pt layer is 90°. If the

barrier layer was in fact present, this would represent a singularity in the electric field distribution during anodization. Therefore, it appears clear that the use of the Al/Pt/Si structure both prevents the formation of an interfacial oxide layer and provides *in-situ* removal of the alumina barrier layer. The mechanism for the barrier layer removal is believed to be field-enhanced dissolution of the alumina and is caused by the termination of the electric field at the Pt layer. Therefore, since the resistance of the substrate and electrolyte is negligible, all the potential drop must occur across the barrier layer. Finally, after the barrier layer is removed, an electrolysis reaction occurs resulting in the generation of hydrogren and oxygen. This is believed to be the cause of the noise observed at the end of the Al/Pt/Si anodization process.

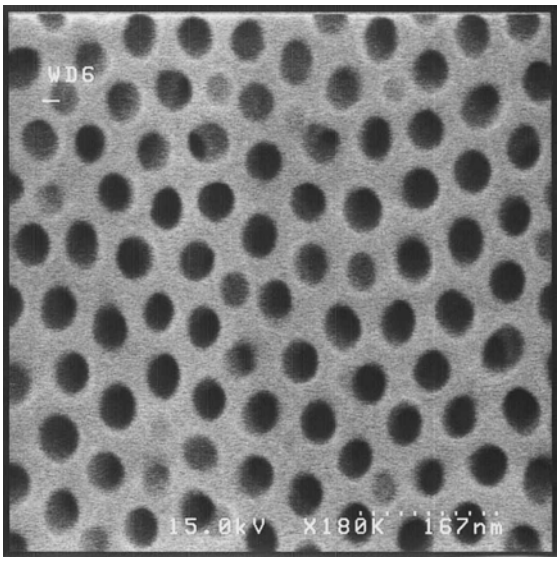

Figure 2-8: Top view of alumina pores formed on the Al/Pt/Si structure.

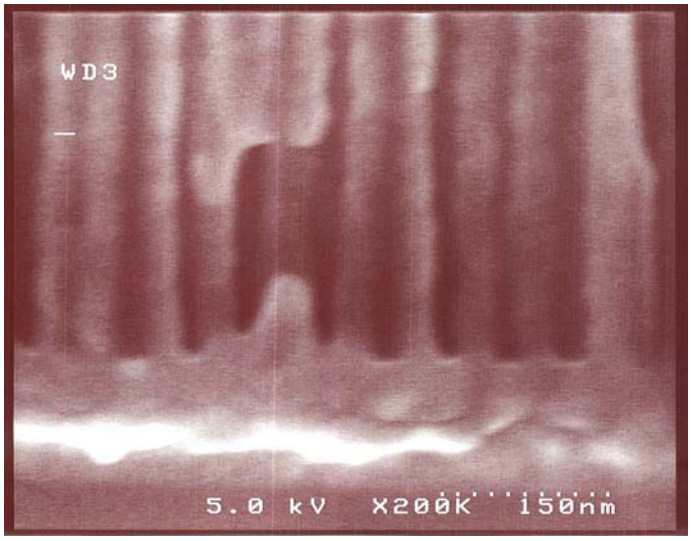

Figure 2-9: Cross-sectional image showing pores contacting the Pt layer.

The *in-situ* removal of the barrier layer with the Pt/Al/Si structure is a very significant result and was presented at the 2001 Electronic Materials Conference in South Bend, IN. This simplifies the problem of ensuring reliable electrical contacts to the semiconductor nanostructures, and enables the use of direct-current (DC) and under-potential (UP) deposition techniques. As will be shown in Chapter 3, the use of these electrochemical synthesis techniques can substantially enhance semiconductor material quality.

2.3 Standard Process Flow

The basic process flow for the fabrication of an alumina thin film directly on a silicon substrate with a single anodization step is described on the following pages:

Substrate Cleaning

2" p-type Si wafers with {100} orientation and 1-3 Ω-cm resistivity are used as the substrate for template formation. These wafers are then cleaned using SummaClean for 30 minutes at a constant temperature of 60° C. This step removes organic and heavy ion contamination. Then, any native oxide is removed with a 3 minute dip in 100:1 HF solution at room temperature. After a 10 minute rinse in DI water (18.2 Ω-cm), the substrates are dried with N_2 and baked at 130° C for 30 minutes to remove moisture.

Contact Formation

A back contact (170 nm) is deposited by magnetron sputter deposition using an 8" 99.999% Al main target at 1kW deposition energy for 3 minutes. The base pressure before sputtering is typically $5x10^{-6}$, and the Argon flow rate is 100 sccm. After deposition, the back contact is annealed at 450° C for 30 minutes in an N_2 atmosphere to ensure an ohmic contact and to enhance film adhesion.

Template Aluminum Formation

Immediately after the back-contact anneal, the substrate is placed in the CVC Magnetron Sputter system and the system is pumped to a base pressure of less than $1x10^{-6}$. Deposition is carried out using the Al main target at an energy of 1kW. The deposition time is dependent on the thickness required for the final alumina template. After deposition, the substrate is annealed at 400° C for 30

minutes in an N_2 atmosphere. The purpose of this step is to improve film adhesion. This does not appear to be required for prime silicon wafers, however it does eliminate the likelihood of adhesion problems when using test silicon wafers.

Anodization

After the wafers have cooled, they are scribed and cleaved to form four separate samples for anodization. The anodization solution is 20% (v/v) H_2SO_4 prepared by dilution from 98% double-distilled sulfuric acid. The acid is then chilled using a Masterflex peristalsis pump and Julabo chiller until the acid reduces a final temperature of 3° C. The temperature of the bath in the chiller at this point is -9° C. The sample is then mounted in a custom designed Teflon apparatus [111] and inserted into the anodization solution. Anodization is then performed at either a constant current density (10-40 mA/cm^2), or at a constant voltage (10-30 V). After the anodization is complete, the sample and apparatus are removed and rinsed in DI water for 10 minutes. The sample is then removed, rinsed in DI water, and dried with N_2.

Pore Widening

To enhance etch uniformity, the sample is soaked in DI water for 12 hours before pore widening. The sample is then pore widened in a 5% phosphoric acid solution for 6 minutes. After the etch, the sample is removed, rinsed in DI water for 10 minutes, and dried with N_2.

2.4 Template Characterization

The alumina templates have currently been characterized by imaging, electrical and optical techniques. The specific results are discussed on the following pages:

2.4.1 Imaging

Imaging of the template material is difficult due to the combination of three factors. First, the features of interest (pores) have diameters down to 4 nm. Second, the presence of pores in the template means that there is a relatively large height variation within the samples. Finally, alumina is a strongly insulating material. The combination of factors restricts imaging to the use of field emission scanning electron microscopes (FESEM), atomic force microscopes (AFM), and transmission electron microscopes (TEM).

TEM

An early TEM image of pores on a silicon substrate is shown in Figure 2-10. While this technique provides the highest feature resolution, sample preparation requirements and expense limits its usefulness for routine template characterization.

FESEM

It has been determined that the optimum instrument for template imaging is the LEO 1530 FESEM that contains a Schottky type (ZrO-W) field emission source. This source provides the high beam brightness and low energy spread seen with cold-cathode field emission sources, while still

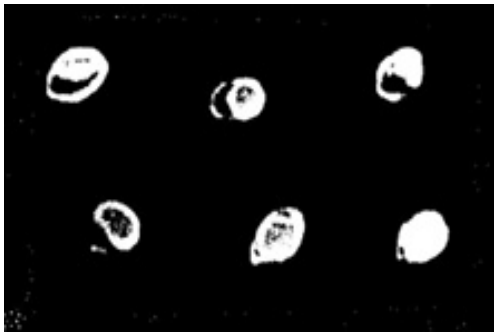

Figure 2-10: TEM image of pores in alumina. Average pore diameter is 13 nm.

providing low beam noise (1%), and low emission current drift (< 0.5%/hour). The field emission gun in the LEO 1530 uses a crossover-free electron path that maintains a high beam energy through the entire electron optical column. The electron beam is decelerated to the desired energy after the beam has passed through the scanning system. The combined effect of the crossover-free beam and the high beam energy minimizes statistical Coulomb interactions and transverse chromatic aberration at low beam energies. This provides a significantly increased resolution for low beam energies (2.5 nm at 1 kV). The magnification of this instrument is continuously variable between 20X to 900,000X, with an accelerating voltage adjustable between 200 V to 30 kV. A representative image from the LEO 1530 is shown in Figure 2-11.

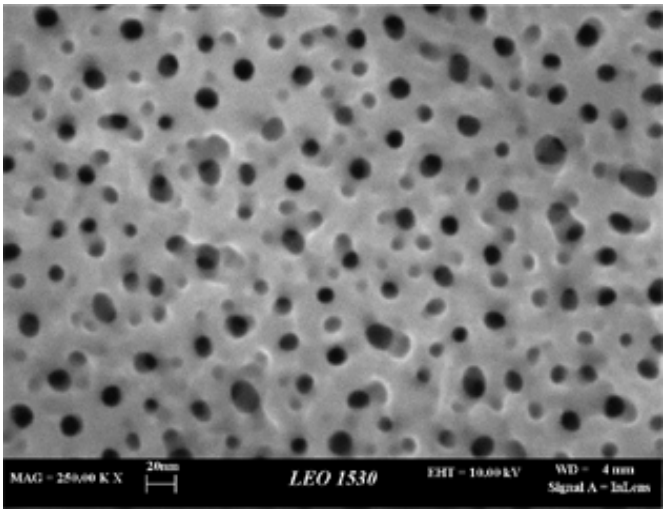

Figure 2-11: LEO 1530 FESEM micrograph showing pores in an alumina template (not pore widened.)

In addition to the LEO 1530, a Hitachi 4500 cold cathode FESEM was used for work at the University of Notre Dame. The cold cathode can provide theoretically higher resolution than the LEO 1530, however this results in a significantly larger beam current density that increases charging in insulating materials. In addition, a cold cathode filament requires substantially lower vacuum pressure ($<1x10^{-10}$) that can degrade instrument performance in a multi-user environment. A representative image from this instrument is shown in Figure 2-8.

AFM

An image obtained using a Digital Instruments Atomic Force Microscope (AFM) is shown in Figure 2-12. It has been determined that the use of tapping mode provides the best images with this instrument due to the large surface topography. As a result of this topography, this technique does not provide the same image quality as an FESEM. However, it is valuable for providing quantitative surface roughness information, primarily for the starting aluminum films.

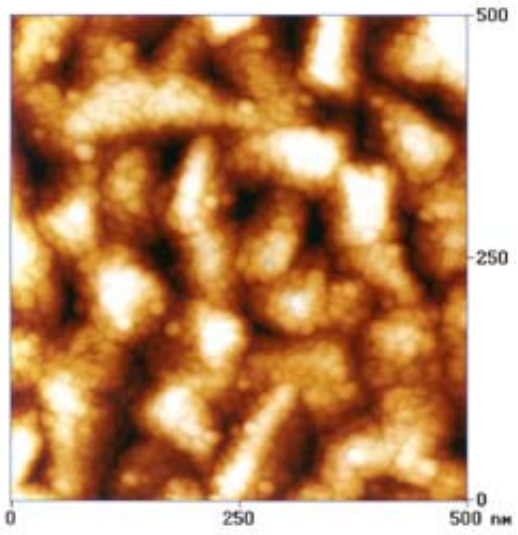

Figure 2-12: AFM image of an alumina template.

2.4.2 Electrical Characterization

By the deposition of a metal top contact to the alumina template, a metal-insulator-silicon (MIS) structure can be formed. Since this type of structure is sensitive to the insulator/semiconductor interface as well as to ionic charge in the insulator, it can be used to characterize average template properties. The characterization of alumina templates by CV analysis was carried out by the deposition of an array of aluminum top contacts on an alumina template by sputter deposition through a shadow mask. An image of a sample with the deposited top contacts is shown in Figure 2-13. After contact deposition, the current-voltage characteristics of the pads was evaluated to ensure that leakage current was below acceptable levels. Then, the capacitance was measured as a function of applied voltage using an HP LCR meter in collaboration with Christopher Garman. A typical CV scan is shown in Figure 2-14.

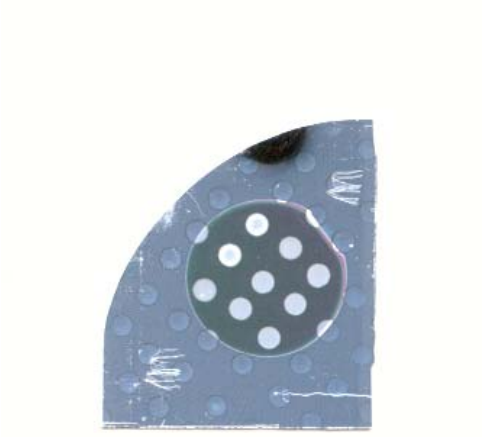

Figure 2-13: A typical sample for CV measurements. Small circular pads are aluminum top contacts.

To investigate the effect of pore widening on the alumina templates, C-V analysis was performed on a set of silicon wafers as a function of current density and pore widening. Then, from the observed C-V behavior, the flat-band voltage was determined. A graphical representation of this analysis shown in Figure 2-15 demonstrates that pore widening significantly reduces the distribution in flat-band voltages. The most likely explanation for this behavior is that pore widening removes the non-uniform pore nucleation layer from the templates.

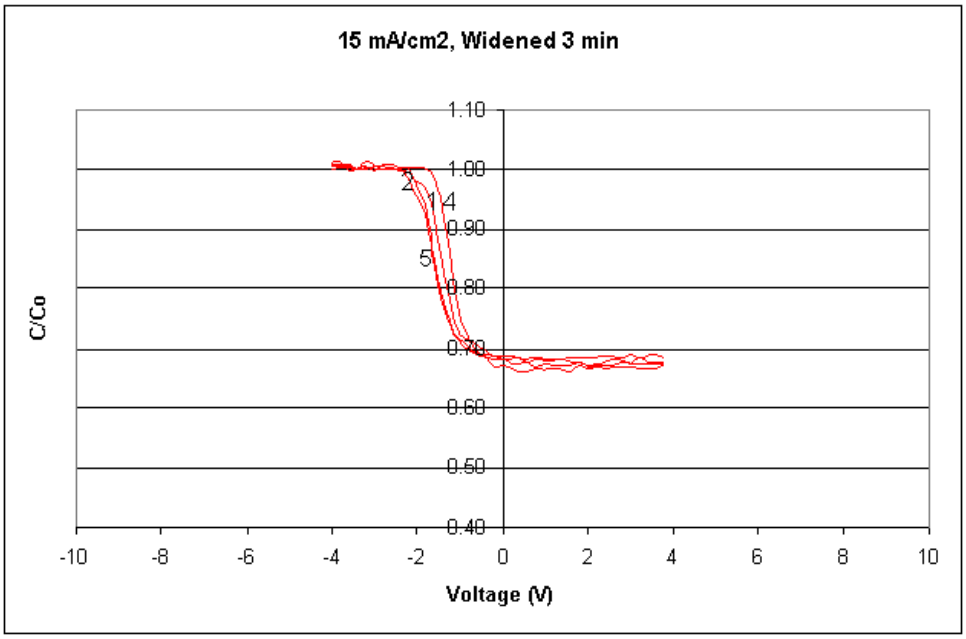

Figure 2-14: A typical Capacitance-voltage characteristic for the template.

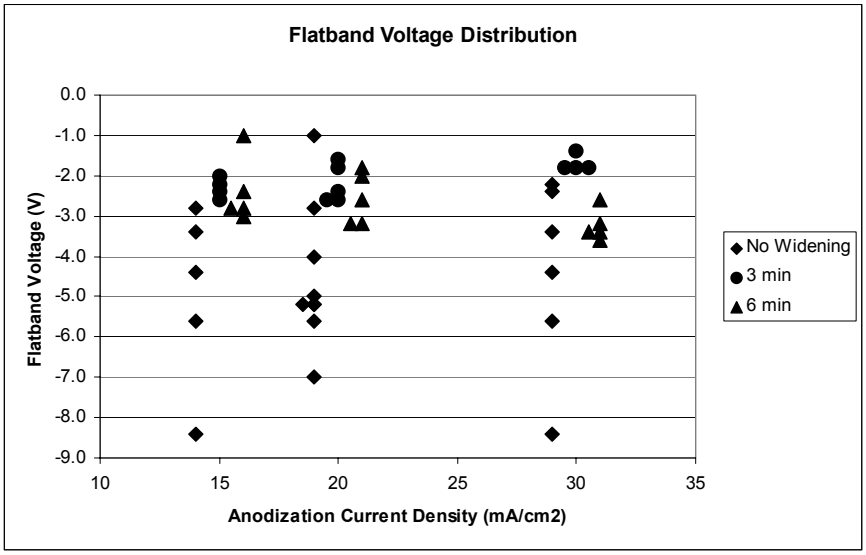

Figure 2-15: Flatband voltages obtained from CV data of pore-widened and pore-unwidened samples.

2.4.3 Optical Characterization

Photoluminescence characterization of alumina templates has been previously shown to result in emission at approximately 460 nm and has been attributed to the incorporation of inorganic anions within the alumina pore sidewalls [99]. Since CV characterization shows a reduction in flatband voltage with pore widening, the effect of pore widening on the alumina template PL was investigated. PL was performed at the Department of Physics at West Virginia University at 5 K and with an excitation wavelength of 325 nm. The results are shown in Figure 2-16. These results show a blue-shift in PL peak wavelength and an increase in emission intensity with increased pore widening. The mechanism for this behavior is not yet clear. However, it has been observed that in the case of porous silicon, storage in Fluroware containers results in blue emission with a narrow spectral range. This is attributed to the outgassing of trace amounts of hydrocarbons that are then

absorbed in the large surface area material. This may provide an explanation for the observed PL data. The samples for this investigation were stored in Fluroware. In addition, pore widening is known to result in an opening of the tops of the pores, resulting in increased surface area. This can be investigated more thoroughly by performing FTIR characterization and looking for the signature absorption bands of CH_3 and CH_2 at between 2939 and 2965 cm^{-1} [112].

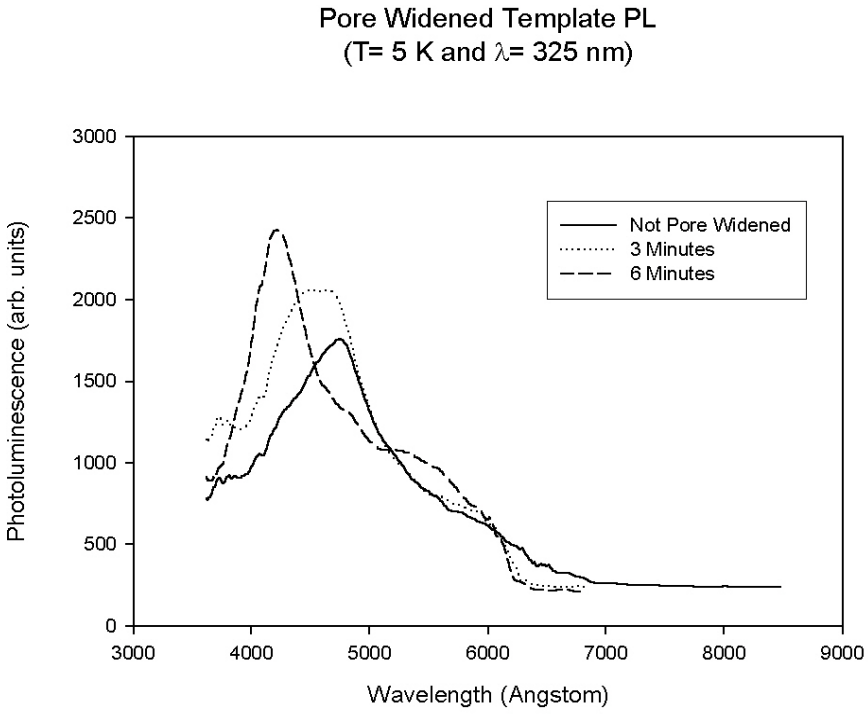

Figure 2-16: Photoluminescence characterization of pore-widened templates.

2.5 Silicon Carbide

The ability to selectively synthesize carbon nanotubes on a silicon carbide substrate is currently being investigated in collaboration with the NASA Glenn Research Center. To accomplish this, it is necessary to be able to deposit a periodic array of Ni dots on the silicon carbide substrate. As part of this effort, the ability to form a template on silicon carbide was verified, and Ni was electrochemically deposited into the template pores. A potential time characteristic for the template formation is shown in Figure 2-17 and an FESEM image of nickel deposited into an alumina templates is shown in Figure 2-18.

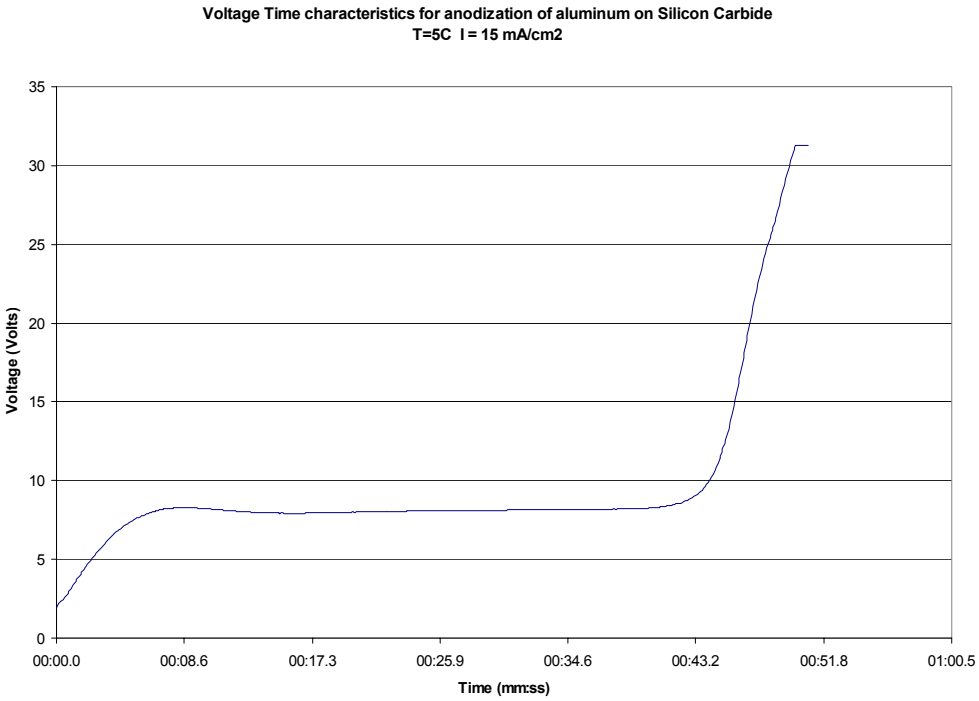

Figure 2-17: A typical voltage-time curve for the anodization of aluminum on SiC substrate.

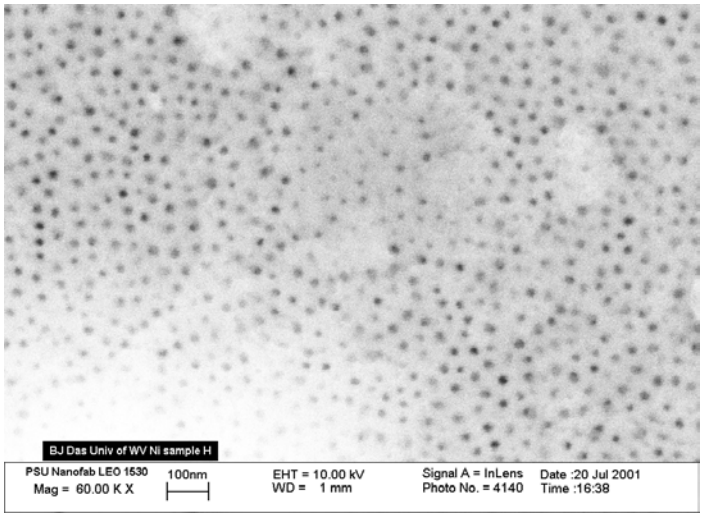

Figure 2-18: FESEM top image of nickel deposited in the pores of alumina thin film template

Chapter 3

Electrochemical Synthesis

Electrodeposition of semiconductor material is a particularly attractive technique since it is possible to fabricate uniform films over a large area with low cost, high throughput, and scalability [113]. In addition, the ability to fabricate compositionally modulated or nonequilibrium alloys raises the possibility of fabricating non-traditional semiconductor materials [114]. Finally, for the special case of nanostructure fabrication using alumina templates, the presence of an applied electric field allows enables the filling of high aspect ratio pores.

In this chapter, the use of electrochemical techniques for the fabrication of semiconductor nanostructures will be discussed. In addition, characterization results for the synthesis of CdS quantum wires using these techniques will be presented.

3.1 Chemical Deposition

The most basic method of semiconductor synthesis in the alumina template pores is referred to as the "Miller" process and was developed at the University of Notre Dame in the early 1990's. In this approach, after template formation, a small AC current is applied to the template to deposit a layer of sulphide ions along the pore walls. Then, the templates are immersed in the appropriate salt solution (i.e. $CdCl_2$) at 100^o C. Chemical analysis indicates the presence of both species (Cd, S) in the pores. However, photoluminescence characterization reveals a very broad emission spectrum. It is the current belief of the developer of this technique that at best only a thin film of CdS is formed

along the pore walls due to the limited supply of sulphide ions. However, this technique is still used by Bandyopadhyay at the University of Nebraska [115].

3.2 Nonaqueous AC Deposition

The primary method of semiconductor deposition into alumina templates formed on bulk aluminum substrates is nonaqueous AC deposition. Nonaqueous techniques are the method of choice for semiconductor deposition since they allow a greater flexibility in the choice of chemical precursors, do not etch either the substrate or deposited material, and avoid the generation of hydrogen through electrolysis of water [113]. The primary solvent used for nonaqueous deposition of II-VI semiconductor material is Dimethyl Sulfoxide (DMSO).

The deposition of II-VI quantum wires into alumina templates using AC deposition was systematically investigated by Moskovits starting in 1996 [116, 117]. In their deposition method, $CdCl_2$ and elemental sulphur are dissolved in DMSO. The material is then deposited at a temperature ranging from between 100-160 C with an applied AC current. The use of an AC current is required due to the presence of the alumina barrier layer. From his investigation, Moskovits was able to conclude that:

1) Uniform CdS quantum wires were formed without the presence of structural voids. In addition, the quantum wires synthesized retained the template pore dimensions.

2) Oriented growth of CdS occured with the c-axis phase of the hexagonal wurtzite phase aligned normal to the substrate surface.

3) Electrochemical deposition into the alumina template increased CdS crystal order and reduced strain when compared with CdS deposition on a bulk Pt electrode.

In his work, Moskovits concludes that the presence of nanometer scale pores results in electrochemical growth from a single nucleation site due to the small pore diameter.

While Moskovits concentrated on structural characterization of the CdS synthesized in the templates, he did not perform optical characterization of the material. Therefore, CdS was synthesied in an alumina template with dimensions of 15 nm and 40 nm by the technique discussed earlier in this section. FESEM images with the templates partially and completely removed by a 10% NaOH etch are shown in Figures 3-1 and 3-2 respectively.

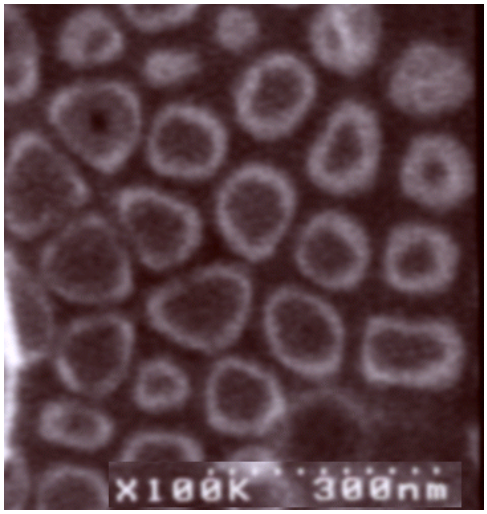

Figure 3-1: FESEM Image of 40 nm CdS quantum wires with alumina template removed.

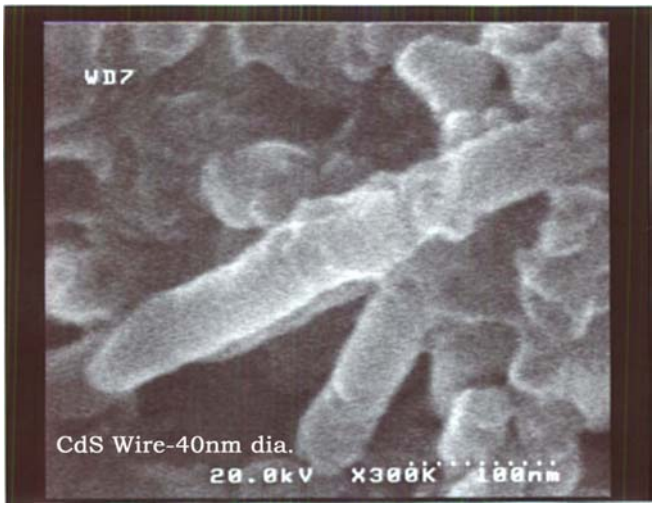

Figure 3-2: 40 nm CdS wires with the alumina template completely dissolved.

The CdS templates were then characterized by low temperature (5 K) photoluminescence and Raman measurements by Lijun Wang in the Department of Physics at WVU. The PL results shown in Figure 3-3 indicate intense luminescence with a relatively narrow spectral range with a peak energy below the bandgap. At peak position the 40 nm wire luminescence is less intense and shows emission that is consistent with the band-edge of CdS. The luminescence from the 15 nm wires is more intense and the below band-gap feature shows structure with what appears to be a doublet. There is no evidence of significant band-edge luminescence in this sample. There does not appear to be a shift in PL peak position between the two samples.

Raman measurements were taken with the 514.5 nm output from an argon ion laser and the beam was focused to a spot size of approximately 10 microns. The results are shown in the range of 300 cm^{-1} in Figure 3-4 and between 1000 to 4000 cm^{-1} in Figure 3-5. There is a significant enhancement in Raman scattering for the sample with 15 nm diameter at the value of the first LO phonon in CdS (300 cm^{-1}). Weak scattering is observed for the 40 nm sample at approximately 313 cm^{-1}. The

decrease in the first LO phonon position with decreasing wire size is consistent with the measurements of Moskovits who reported a shift from 308 cm^{-1} to 300 cm^{-1} for wires with dimensions less than 10 nm. It is important to note here that the quoted values for quantum wire size of 15 nm and 40 nm is based on measurements of the template pore diameter, rather than actual wire diameter. In the case of Moskovits, quoted dimensions are actual quantum wire size.

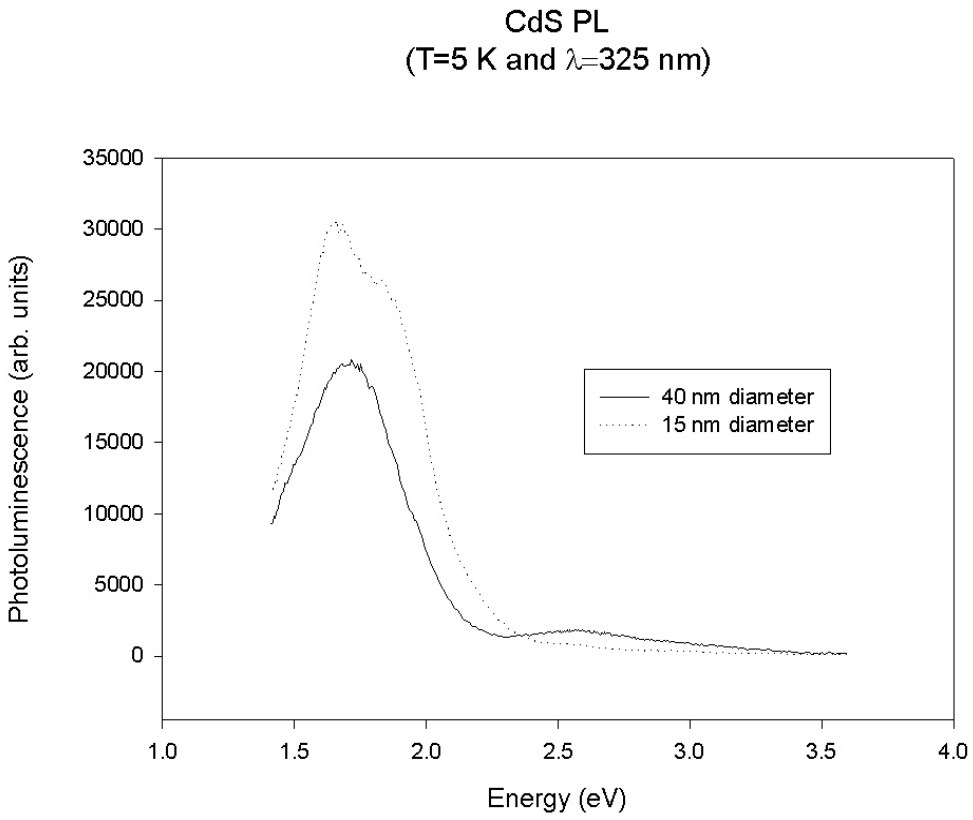

Figure 3-3: PL characterization of CdS wires with diameters of 40 and 15 nm.

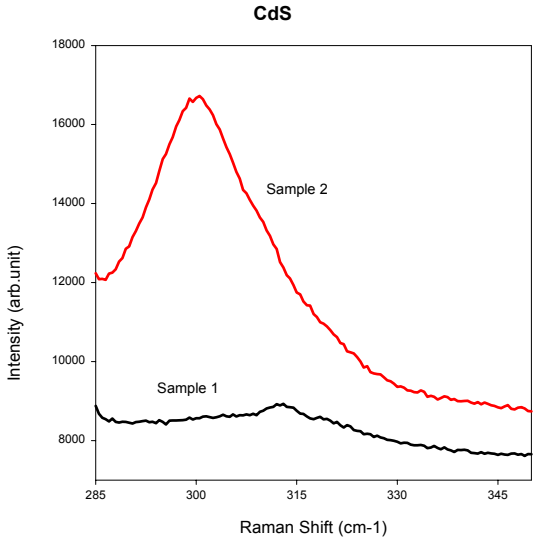

Figure 3-4: Raman shift of CdS quantum wires with 15 nm (Sample 2) and 40 nm (Sample 1) diameter near the first LO phonon.

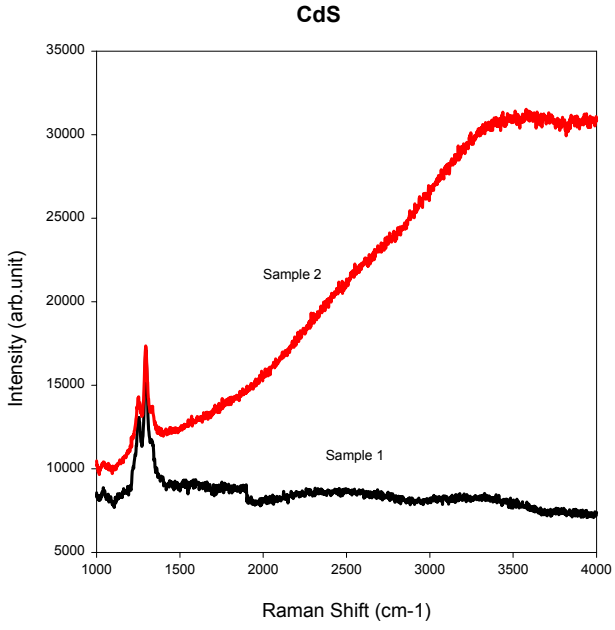

Figure 3-5: Raman shift of CdS quantum wires with diameters of 40 nm (Sample 1) and 15 nm (Sample 2).

The broad peak in the range between 1000-4000 cm^{-1} was observed by Balandin in samples fabricated using the deposition technique discussed in Section 3.1 and was attributed to inter-subband transitions in CdS quantum dots. This feature is not observed in the 40 nm sample and therefore may indicate the onset of quantum confinement for the 15 nm diameter sample. The series of sharp lines around 1300 cm^{-1} has been attributed by Giles and Wang to luminescence from trace amounts of rare earth impurities.

3.3 DC Nonaqueous Deposition

Direct current (DC) deposition of CdS, CdSe and CdTe into alumina templates was recently investigated by Xu [118]. This was enabled by fabrication of an alumina template on a bulk substrate, removing the template by dissolving the barrier layer in $CuCl_2$, and depositing silver on the base of the template by thermal evaporation. By removing the barrier layer, this approach enabled the use of a DC deposition technique. Deposition was preformed using the DMSO technique discussed above with a constant current of 1.0-1.5 mA/cm^2. An HRTEM image is shown in Figure 3-6 that indicates the presence of single crystal material.

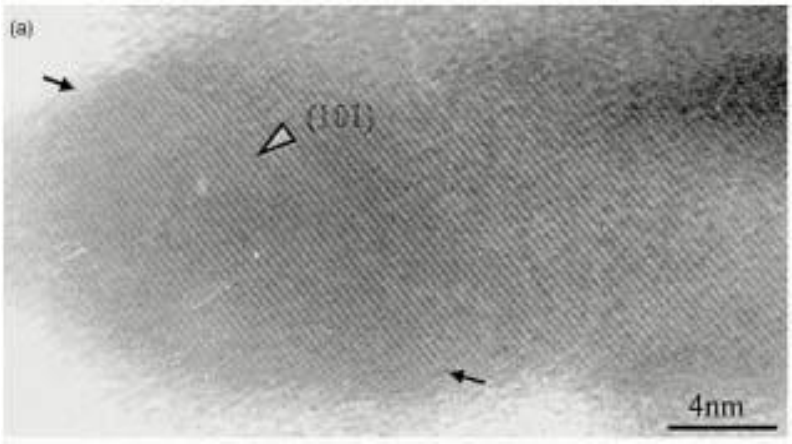

Figure 3-6: HRTEM Image of a 20 nm CdS quantum wire. (After Xu).

While the work of Xu demonstrates the promise of the DC deposition technique, the experimental method used is not viable for efficient material fabrication. However, the *in situ* removal of the alumina barrier layer with the Al/Pt/Si structure demonstrated in Chapter 2 enables DC synthesis of semiconductor material using a silicon substrate.

Chapter 4

Silicon Nanostructure Fabrication

The ability to fabricate compound semiconductor nanostructures by electrochemical deposition into an alumina template was demonstrated in the previous chapter. However, the alumina template can also be used as a pattern transfer mask for the formation of nanometer scale structures in a substrate material. To explore this approach, three methods for nanostructure formation on a silicon substrate have been identified. These three approaches (electrochemical formation of porous silicon, plasma etching of nanoscale silicon pores, and etching of silicon quantum pillars) are discussed in the remainder of this chapter.

4.1 Template Based Formation of Porous Silicon

Porous silicon has been used since the 1950's in electronic applications (insulators, gettering, sacrificial layers, etc.) [119] however, it was not until the observation of intense, room temperature red photoluminescence from this material by Canham [120] in 1990 that substantial research into the properties of this material began. Despite this research effort, practical photonic device applications have been limited by the broad emission spectrum and the fragile nature of the material. To address these issues, the ability to from porous silicon through a preformed alumina template was investigated. This approach can provide the advantages of initial ordering for porous silicon formation, as well as providing an *in situ* encapsulation layer through hydrolysis of the template. An experimental plan was developed to verify first that porous silicon could be formed by an

alumina template, and second that the template would remain intact during anodization. In the remainder of this section, an overview of the properties of porous silicon will be presented, along with a description of the fabrication techniques used and the results of photoluminescence characterization of the resulting structures.

4.1.1 Porous Silicon

Porous silicon is formed by anodic etching of a crystalline silicon substrate in a solution of hydrofluoric acid (HF). The resulting structure can be characterized as an intertwined network of free standing nanoscale (1-4 nm) structures with substantial inhomogeneity in both size and shape. While a detailed theoretical model for porous silicon formation remains elusive, it is generally agreed that the basic mechanism involves anodic oxidation of the silicon substrate with subsequent etching of that oxide in the HF solution [119].

The primary optical characterization method for porous silicon is low temperature (4.2 K) and room temperature (300 K) photoluminescence. These measurements have detected emission ranging from the UV at 350 nm [121] to the infrared at 1500 nm [122]. In between these extremes, emission in the range of 400-800 nm ("S Band"), and at approximately 470 nm ("F Band") has been detected. The emission at 470 nm is only observed in oxidized porous silicon samples and is believed to result from the formation of a contaminated or defective silicon dioxide layer on the nanostructures [122, 123]. Infrared emission has been observed only after annealing under UHV conditions and is currently believed to result from dangling bonds at the nanostructure surface [124]. Ultraviolet emission is only observed from oxidized layers and is believed to result from defects in the oxide layer [125]. It is important to note these emission bands are distinct from the weak band-edge luminescence observed at low temperature (4.2 K) in crystalline silicon through TO-phonon assisted radiative recombination [122].

Emission in the range of 400-800 nm has received the most attention since this has been experimentally shown to be the most stable luminescence and since it is believed to result from quantum confinement effects in the silicon nanostructures. For this luminescence to occur, it has been experimentally demonstrated that a critical threshold of porosity must be obtained (between 70 and 80 %) [122]. This observation can be explained within the quantum confinement model by noting that for luminescence to occur, the nanostructure confinement length must be less than the bulk Silicon exciton Bohr radius of 5 nm [126]. For this and other reasons, it is generally accepted that the quantum size effect is the dominant mechanism for the observed "S-Band" photoluminescence. A detailed discussion of the experimental evidence to support this view is provided in Appendix A.

In additional to the experimental evidence, recent theoretical work has shown that the observed red photoluminescence is consistent with a change in the silicon band structure resulting from quantum confinement. In particular, work by Horiguchi has verified that the effective mass approximation is valid for silicon quantum wires with dimensions down to 1 nm [127]. Using this result, he has shown that for quantum wires fabricated on the {100} surface of crystalline silicon, the minimum energy of the one dimensional conduction sub-bands shift from near the X-point to the Γ-point, regardless of wire shape [128]. Since the valence band maximum remains at the Γ-point regardless of nanostructure size, this observation confirms that silicon quantum wires with characteristic dimension less than the bulk exciton Bohr radius behave as a direct band-gap material. As a result, no-phonon transitions are allowed in these silicon quantum wires, leading to an enhanced radiative recombination rate.

A recent combined experimental and theoretical investigation has revealed that the photoluminescence properties of porous silicon are strongly influenced by the dielectric constant of

the medium surrounding the quantum wires [129]. As the dielectric constant is increased from the vacuum value (ε_d=1), to a value larger than that of silicon (ε_d=11.7) the exciton binding energy decreases by up to a factor of 100. This then results in a marked quenching of PL intensity due to thermal disassociation of the exciton, particularly at room temperature [129]. This result is significant since it provides increased evidence that quantum effects are responsible for the observed luminescence, and indicates that the encapsulation of the silicon nanostructures can substantially effect nanostructure optical properties.

4.1.2 Experimental Method

An experimental investigation was conducted to determine the viability of using an alumina layer as both a template for porous silicon growth and as an encapsulation layer for porous silicon. This investigation consisted of two parts. The first part was to evaluate the ability to fabrication porous silicon through an alumina template and to determine the effects of the template on the porous silicon optical properties. The second part was to verify that alumina remained intact during porous silicon formation and to determine the effect of alumina pore sealing on the PL characteristics of porous silicon. For both investigations the starting material was a 0.1-0.3 Ω-cm {100} p-type silicon wafer. For all devices a 400 nm Al-Cu alloy was deposited on the back surface by magnetron sputter deposition. The back contact was then annealed at 450 C in a nitrogen atmosphere for 30 minutes to provide good metal adhesion and to reduce the contact resistance. At this point the wafers were separated into different lots for specific processing.

One set of wafers was designated to be used to fabricate porous silicon on the bare substrate surface. The second set was designated for alumina template fabrication and 170 nm Al-Cu alloy was deposited by magnetron sputtering. The alumina templates were then formed by anodization in 20%

sulfuric acid at a current density of 20 mA/cm^2. Each template was then paired with a bare silicon substrate for porous silicon formation. Porous silicon was formed by anodization in a (4:1:1) solution of DI Water, Ethanol, and 49% HF for 30 seconds at current densities of 25, 40, and 60 mA/cm^2. One sample at 40 mA/cm^2 was then hydrolized in 100 ^{o}C DI water for 10 seconds to partially seal the template pores. A cross-sectional view of the material structure is shown in Figure 4-1.

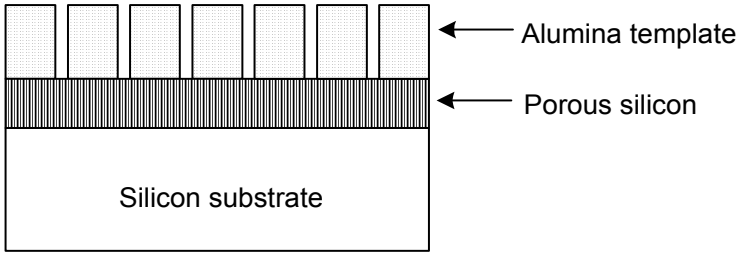

Figure 4-1 Schematic cross-section showing the formation of porous silicon through the pores of an alumina template

4.1.3 Characterization

Photoluminescence characterization was performed at the Department of Physics at West Virginia University at temperatures ranging from 5 to 300 K and an excitation wavelength of 325 nm. The results of this characterization are shown in Figures 4-2, 4-3, and 4-4 and reveals that porous silicon was formed in all samples. The PL peak positions show a red-shift with decreasing anodization current density of 580 nm (60 mA/cm^2), 620 nm (40 mA/cm^2), and 700 nm (25 mA/cm^2). In all cases, the samples with an alumina template show increased PL emission when compared with the bare porous silicon samples. For samples anodized at 60 and 40 mA/cm^2 there appears to be no shift in peak position between samples with and without templates. However, for the sample anodized at 25 mA/cm^2 there appears to be a red-shift of approximately 20 nm in PL peak position.

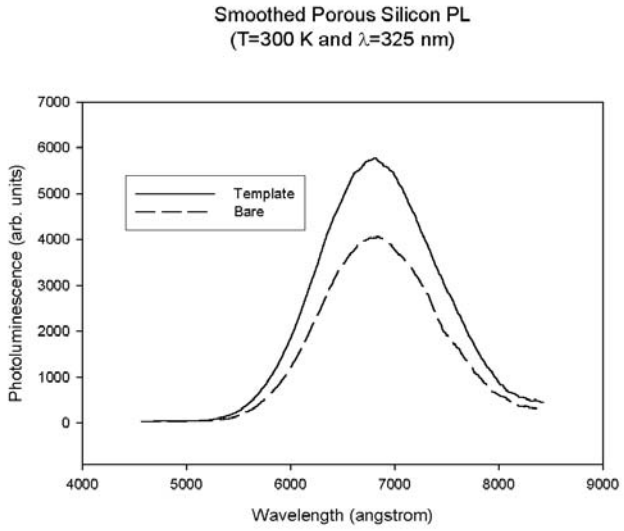

Figure 4-2 Room temperature PL of PS anodized at 40 mA/cm2.

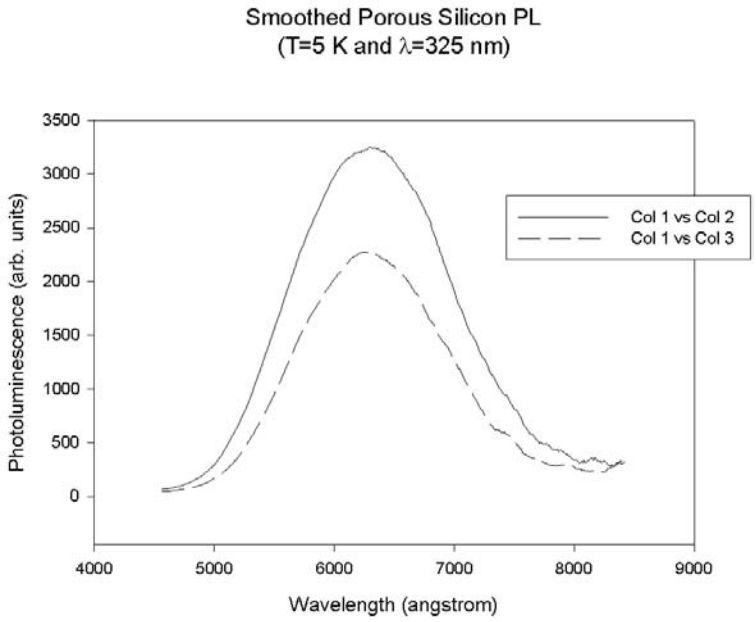

Figure 4-3: Low temperature PL of PS anodized at 40 mA/cm2.

In addition, a top view and a cross sectional image of the partially sealed porous silicon sample were obtained using an FESEM. The cross-sectional image revealed that a porous layer was formed with a thickness of 450 nm. The top view confirms that the alumina template remained intact and is shown in Figures 4-6 and 4-7. To confirm the presence of an alumina template on the other two samples, contact pads were deposited through a shadow mask and the capacitance of the structure was determined. The results of these measurements are consistent with the alumina template remaining at least partially intact.

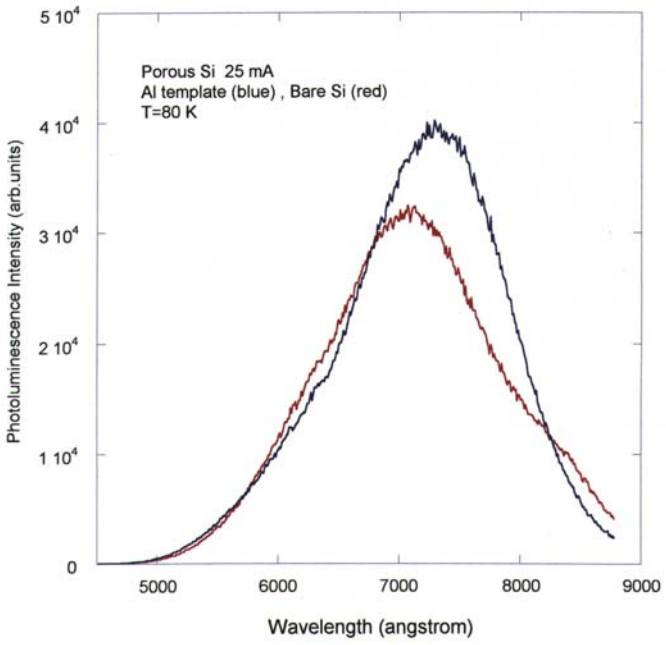

Figure 4-4: PL (80 K) of PS anodized at 25 mA/cm2.

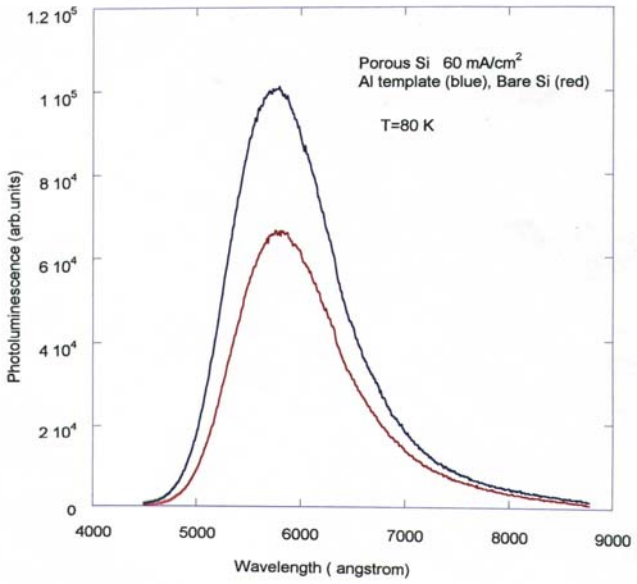

Figure 4-5: PL (80K) of PS formed at 60 mA/cm2.

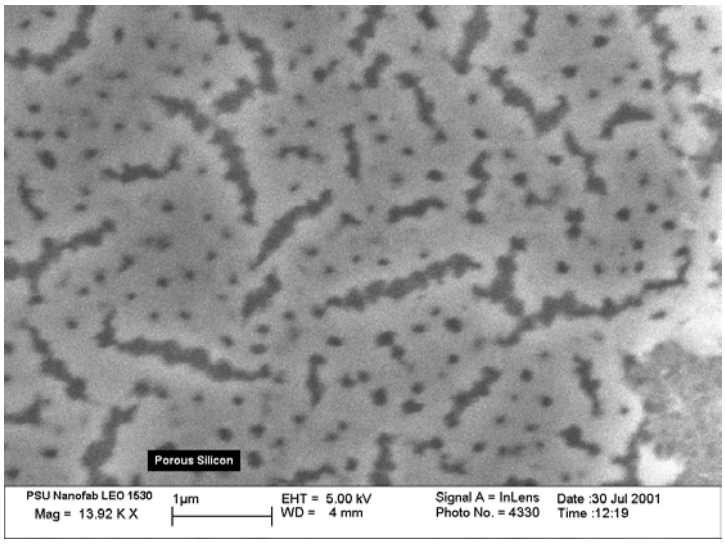

Figure 4-6: FESEM image of hydrolized alumina template after porous silicon formation.

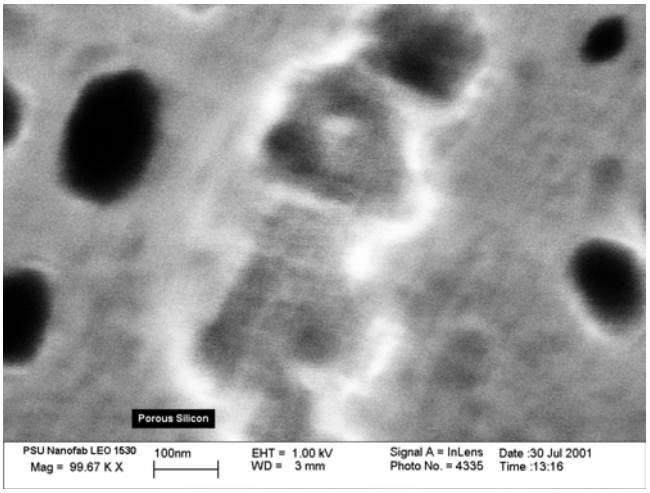

Figure 4-7: FESEM image showing pores remain intact after porous silicon formation.

4.1.4 Analysis

The PL data indicates that porous silicon was formed through the templates even without prior removal of the barrier layer. Alumina is known to be mildly resistant to hydrofluoric acid and with chilling of the anodization solution, significant chemical etching of the template is not expected to occur during the short anodization time (30 s). However, it is reasonable to assume that field assisted dissolution of the barrier layer occurred and led to porous silicon formation. This theory is supported by the images that demonstrate that the alumina template remains intact after anodization. However, it is not clear if the cracking in the template is the result of chemical etching by HF, or is the result of mechanical stress due to the formation of aluminum hydroxide during the sealing process.

The observed PL peak positions are consistent with the nanostructure sizes and porosity expected from the applied anodization current [130]. The fact that there is no shift in PL peak position for samples at 40 and 60 mA/cm^2 tends to indicate that there is no effective variation in average

nanostructure size between samples with and without a template. However, the fact that the sample formed at 25 mA/cm^2 does show a significant shift tends to suggest that there may be a variation in the nanostructure size distribution. If this is correct, the red-shift would indicate that the average nanostructure size for the sample with the template is larger than without a template. It is significant to note that this effect is observed for the sample with the lowest porous silicon anodization current density and therefore the largest silicon nanostructure size. The possibility exists that the closer match between alumina pore size and porous silicon quantum wire size has influenced the anodization process.

The PL data also indicates that samples with a template have higher luminescent efficiency than those without a template. This is not believed to result from the actual emission process but instead appears to indicate enhanced detection of emitted photons during the PL experiment since it has been demonstrated that there is a strong correlation between PL intensity and PL peak position (i.e. an increase in intensity with decreasing emission wavelength) [131]. Therefore, based on the current understanding of the photoluminescence properties of porous silicon, a quantum explanation for the increased intensity would require a blue-shift in emission wavelength. The actual mechanism for the increased photon collection efficiency is not clear. The alumina layer should provide slightly increased absorption of both the incident and emitted photons, as well as increased reflective loss (3.18% for the template, 0.82% for porous silicon alone). Two possible explanations for the increased photon collection efficiency is a "waveguiding" effect due to the air/alumina/PS structure, and/or diffuse scattering of light at the rough alumina/air interface.

Sealing of the template pores by hydrolysis does not appear to negatively effect the optical properties of the porous silicon layer. This implies that aluminum hydroxide is a viable encapsulation material for porous silicon. The next step is to calibrate the hydrolysis process for

complete pore closure. In addition, it would be valuable to quantify any improvements in the long term reliability of porous silicon resulting from the encapsulation layer.

4.2 Pattern Transfer

In the previous section the ability to fabricate porous silicon through an alumina template was verified. In that technique, the template was used as a mask for electrochemical anodization of a silicon substrate to form porous silicon. The viability of using the template to form nanometer scale pores in a silicon substrate was recently demonstrated by collaborators at the University of Notre Dame [132]. In their approach, an alumina template was fabricated on a silicon substrate. The template was then pore widened and the barrier layer chemically removed in phosphoric acid. The template pattern was transferred to the silicon substrate using an Cl_2/BCl_3 reactive ion etch. A cross-sectional FESEM image of the nanoscale silicon pores is shown in Figure 4-8.

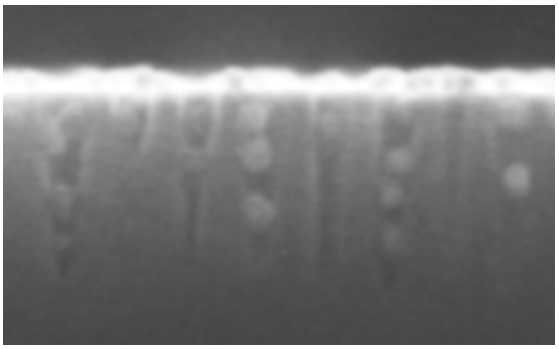

Figure 4-8: Cross-sectional image showing colloidal particles deposited into silicon pores.

This technique is being used to electrophoretically deposit colloidal semiconductor nanostructures into the silicon pores. As a proof of concept, two types of colloidal gold particles were electrophoretically deposited into the nanoscale silicon pores: 15 nm diameter gold particles stabilized by citrate ligand, and 15 nm diameter gold particles with 3 nm thick silica shells [133]. The purpose of using the two different types of colloids was to determine the impact of colloid-

colloid interactions inside the nanopores. Both species deposited into the nanoporous surfaces were found to be mechanically and chemically stable. In addition, the ability to deposit multiple colloids into a single pore was demonstrated. An FESEM image showing the deposited colloids is shown in Figure 4-9. The Electrochemistry Research Group at Notre Dame is currently developing a model of the electric field distribution during electrophoresis to optimize and control the deposition process. The preliminary results of this model indicate that a "self-focusing" phenomenon occurs at the pore surface that helps to guide colloidal particles into the silicon pores.

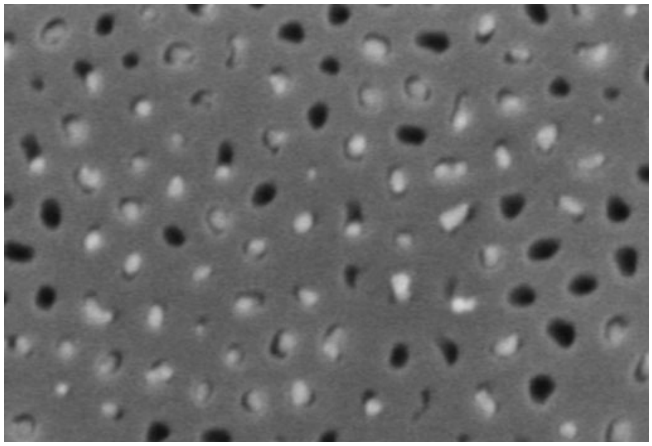

Figure 4-9: FESEM top view showing colloidal particles in silicon pores.

The ability to electrophoretically deposit nanoscale colloidal particles into the pores can be used to fabricate an electro-optic modulator based on the quantum confined stark effect (QCSE). Semiconductor nanostructures have the potential to provide ultra-high performance optical modulators with large modulation depths as well as very high operation speeds. The basis of the expected performance improvements are the strong non-linear and electro-optic effects that occur in low dimensional nanostructures due to quantum confinement. Theoretical investigations of the effect of electric field on the optical properties of semiconductor nanostructures show an enhanced effect with decreasing dimensionality due to the quantum confined Franz-Keldysh effect and the

quantum confined Stark effect (QCSE) [134, 135]. In such systems, when an electric field is applied parallel to the direction of quantum confinement, a red-shift is observed in the absorption edge together with an increase in the absorption coefficient. Thus, if a light beam with photon energy close to the absorption band-edge is transmitted through the material, its intensity can be modulated through the application of an electric field. Since QCSE and Franz-Keldysh effect are quantum mechanical in origin, the optical property modulation caused by it is extremely fast, which is the basis for the high performance enhancement of the modulator. A schematic cross-section of an optical modulator using semiconductor nanostructures is shown in Figure 4-10.

For the specific case of silicon through-wafer optical interconnects, it is necessary to have an active material that can modulate an optical beam with an energy less than the band-gap of silicon (1.11 eV). For most through-wafer interconnect architectures, VCSELs (vertical cavity surface emitting lasers) with an emission wavelength of 1.3 microns (0.95 eV) is used [136]. Due to the blue-shift resulting from quantum confinement, it is necessary to chose a material with a bulk band-gap significantly less than this value. The most promising candidate appears to be InAs with a bulk band-gap of 0.32 eV. For the case of a modulator, where carrier transport is not an issue, colloidal

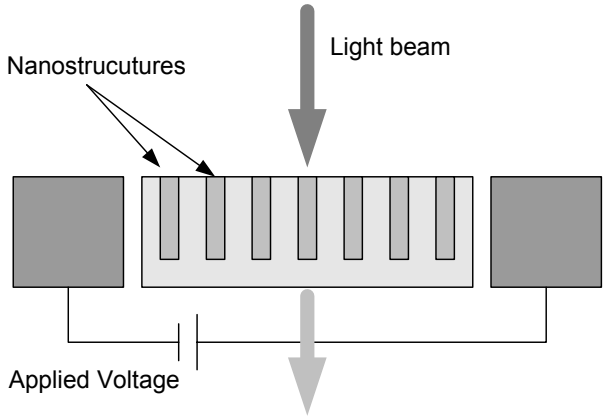

Figure 4-10: Schematic cross-sectional view showing electro-optic modulator based on QCSE.

particles are a viable option. Alivisatos has demonstrated the ability to synthesis InAs colloids with sizes ranging down to 1 nm [137]. As a result, the band-gap of the colloidal quantum dots can be continuously varied from 0.32 eV to 2 eV [138]. Assuming a VCSEL as the source for the through-wafer interconnect scheme, an InAs colloidal size of 3.5 nm will provide modulation of the VCSEL beam.

This concept is currently being partially funded by the National Science Foundation and being investigated as part of a research collaboration with Dr. George Ponchak of the NASA Glenn Research Center. The goal of this collaboration is to fabricate a silicon through wafer optical modulator that is driven by the electric field between two RF microstrip lines. When an RF signal is applied to the microstrip lines, the electric field will modulate the incident infrared beam and be detected using a photodetector mounted above the substrate.

4.3 Silicon Nano-Pillars

In the previous section, the use of an alumina template combined with reactive ion etching to create nanoscale pores in a silicon substrate has been discussed. However, to create silicon light emitting structures, it would be desirable to reverse this process and instead of creating pores to create silicon pillars by RIE. The advantage of this approach compared with the template based formation of porous silicon discussed in Section 4.1 is that direct transfer of an inverse of the alumina template pattern should provide enhanced nanostructure size and shape control resulting in substantially reduced inhomogeneous broadening of the emission spectrum. In addition, since this approach uses a crystalline substrate as the active material, concerns over material quality and unintentional dopant incorporation during electrochemical deposition are relaxed. A schematic of the proposed device structure is shown in Figure 4-11.

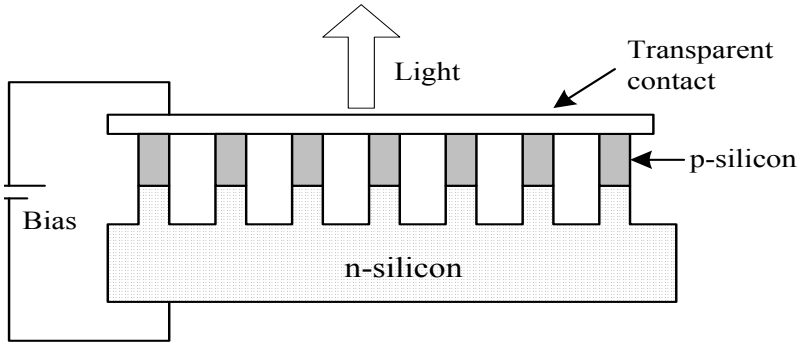

Figure 4-11: Cross-section schematic of silicon nano-pillar light emitting device.

The primary challenge to be addressed in creating this device structure is to develop a process flow to provide image reversal of the template pattern. The initial process flow to accomplish this is provided below:

Template Fabrication

The first step in pillar formation is the creation of a highly ordered alumina template. This is created by depositing 1 micron of 99.999% pure Aluminum by electron beam deposition. The first 500 nm of the aluminum would be anodized at a constant potential of 10 Volts giving a pore diameter of 12 nm [132]. This material would then be etched in a phosphoric/chromic acid solution to remove the template and the process is repeated with an anodization of 400 nm of aluminum. Finally, the last 100 nm of aluminum would be anodized and pore widened to remove the barrier layer (5% H_3PO_4 - 1 hour).

Nickel Electrodeposition

After pore widneing, a nickel plug is electrodeposited into the pores using a standard electrochemical deposition technique as discussed by Garman [111]. The alumina template

is then removed by etching in 0.01 M NaOH for 1 hour leaving an ordered array of nickel dots on the silicon surface.

Silicon Etching

After nickel deposition and template removal, the image reversed pattern is transferred to the silicon susbtrate by reactive ion etching (RIE). There are three primary concerns that need to be addressed in the design of this etch process. First, the etch chemistry must be designed so as to provide an appreciable etch rate and etch selectivity for silicon. Second, sufficient anisotropy must be obtained to prevent substantial silicon pillar size variation down the length of the wire. Finally, the etch process should produce smooth (pillar) side walls. Fortunatley, due to the recent emphasis on silicon deep-trench etching for deep-submicron device isolation, these concerns have been investigated. The use of an ICP-RIE head is used to provide independent control of ion-density and ion-energy resulting in a high etch rate as well as good etch selectivity. The proprietary Bosch-etch process has been demonstrated to proivide good anisotropic etching of silicon by alternating etching and passivation of the silicon sidewalls [139]. Finally, the use of a liqued nitrogen cooled substrate holder mimimizes chemical etching of the silicon resulting in both increased etch anisotropy as well as reducing sidewall roughness.

Oxidation

After pillar formation, the nickel dots are removed by a wet chemical etch. After cleaning, the substrate is oxidized to both reduce damage to the crystalline silicon as a result of the etch process as well as to reduce the silicon pillar size. This process is enabled by the recent observation that oxidation of silicon nanostructurs is a self-limiting process [130].

Therefore, endpoint control requirements during this thermal oxidation step are substantially relaxed.

Contacts

For initial development, characterization of theses structures will be performed by photoluminescence which does not require top contacts to the silicon nanostructrues. However, for the development of an electroluminescent device, the fabrication of ohmic contacts as well as charge transport through the silicon pillars is a critical concern. At this time, the contact material to be used is Indium Tin Oxide (ITO), which is a transparent condutor deposited by reactive sputtering. One concern is that deposition of this material will fill the voids between the silicon pillars. However, based on work with transparent top contacts to porous silicon, this does not appear to be a fundamental limitation.

In summary, a process for the non-lithographic fabrication of orderd silicon pillars has been indentified. This process complements the already developed process for the fabrication of silicon ordered silicon pores.

Chapter 5

Photovoltaic Applications

An emerging application for nanoscale photonic devices is the development of photovoltaic devices for the direct conversion of solar energy into electricity. The use of a nanoscale alumina template has been investigated for both direct fabrication of photovoltaic devices based on compound semiconductor nanostructures as well as for use as an etch mask for surface texturing of silicon photovoltaic cells. These two specific applications are discussed in the remainder of this chapter.

5.1 Multijunction Nanostructure Photovoltaic Cell

For photovoltaic (PV) technology to be a serious contender as an alternative energy source, the electricity generated must be reasonably cost-effective when compared with current fossil fuel sources [140]. This will require both an increase in the efficiency of PV cells as well as a reduction in manufacturing costs. While photovoltaic cells based on bulk semiconductors can provide very high efficiency (e.g. a conversion efficiency of >25% for single junction GaAs cells), the high manufacturing costs of these devices limits their use to primarily space based applications. In an effort to reduce manufacturing costs, photovoltaic cells based on thin film technology have been developed. The most promising thin film technologies for commercial applications are based on (i) amorphous silicon, (ii) cadmium telluride (CdTe), (iii) copper indium diselenide (CIS)/copper indium gallium diselinide (CIGS), (iv) crystalline silicon films, and (v) dye-sensitized TiO_2 cells [140-143]. Amorphous silicon cells are the subject of intense research and development, and this

appears to be a manufacturable technology, however their efficiency remains quite low, usually < 10%, although as high as 11.4% has been observed [144]. Cadmium based cells (CdTe, CdS) have a higher reported efficiency (15.8%), however these materials have poor stability, and are difficult to economically manufacture in large areas while maintaining the required material quality [145]. Copper indium gallium diselenide (CIGS) has shown the highest efficiency (18.8%) for a thin film photovoltaic cell, but manufacturing this complex material at low cost is a difficult task. Crystalline silicon cells have demonstrated efficiencies as high as 24.4% [146], but growing large area thin films economically on a suitable substrate is a major technical challenge [145]. Dye sensitized TiO_2 cells are unique in that carrier generation and collection are spatially separated. These cells can be inexpensively manufactured, but currently have an efficiency of around 11% [147]. In addition, questions remain about the long term stability of the dye sensitized TiO_2 cells , in part due to the difficulty in sealing the material from the elements. To attempt to alleviate these limitations, the feasibility of using electrochemically self-assembled semiconductor nanostructure arrays as the building block for manufacturable, high efficiency solar cells is being investigated with the support of the National Renewable Energy Laboratory (NREL). Since this approach uses a non-vacuum fabrication technique and is based on an established industrial process, the requirement for manufacturability and low production cost can be met. In addition, due to quantum confinement effects a relatively high photovoltaic efficiency is expected to be obtained.

Nanostructure based PV cells have been previously proposed due to their potential to provide a very high energy conversion efficiency [114]. This large energy conversion efficiency results from the following effects: (a) nanostructure *crystallite sizes* are comparable to the *carrier scattering lengths*, this significantly reduces the carrier scattering rate, thus *increasing the carrier collection efficiency*; and (b) the *strong absorption coefficient* of nanostructures due to the increased density of states. In addition, by varying the size of the nanostructures, the band gap can be tuned to absorb in a

particular photon energy range [114]. However, to achieve these advantages for non-cryogenic temperatures, it is necessary to fabricate periodic arrays of individual nanostructures with a uniform size below 20 nm. This maximum size is determined by the requirement that the energy separation of discrete levels due to quantum confinement be greater than the associated thermal broadening. As was demonstrated in Chapters 2 and 3, the alumina template technology can be used to form II-VI semiconductor quantum wires with dimensions less than 20 nm. In addition, due to the ability to create multiple layers of nanostructures, it is possible to implement multijunction photovoltaic cells. In the multijunction concept [148] photovoltaic cells with multiple layers of semiconductor material are fabricated. Each layer of semiconductor material is chosen to optimize absorption in a discrete section of the solar spectrum, thus maximizing total photovoltaic cell efficiency. This approach is particularly well suited for nanostructure-based photovoltaic cells since each layer of semiconductor quantum wires will have maximum absorption in a relatively narrow spectral range. By varying either the diameter of the wires, and/or the chemical composition, the maximum absorption peak can be varied across a wide section of the solar spectrum.

A cross sectional diagram of the proposed multi-junction photovoltaic cell architecture is shown in Figure 5-1. The substrate material (plastic, glass) is application specific and is chosen to meet economic, encapsulation, or mechanical requirements. The back contact is either metallic (Platinum) or a transparent conducting oxide (Indium Tin Oxide). The thickness of the alumina template is optimized to balance absorption, transparency (for the multijunction cell), and carrier transport. The top contact layer is a transparent conducting oxide such as ITO. In the case of a multijunction cell, a transparent insulating material (silicon nitride) is used to provide electrical isolation between the active layers and to serve as an additional barrier layer for ionic contamination.

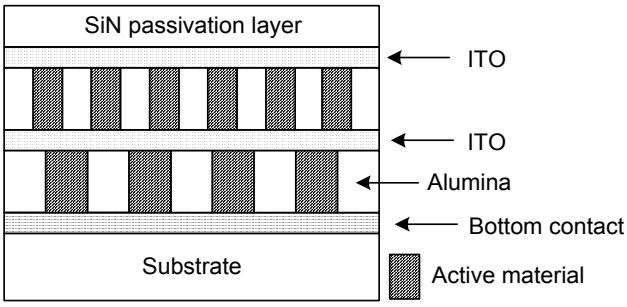

Figure 5-1 Schematic cross-section of a multi-junction photovoltaic cell

5.1.1 Analysis

At this stage, the primary focus of the photovoltaic research effort is to fabricate and characterize individual nanostructure layers. As one part of this effort, the degree to which quantum confinement and alloying can cover the solar spectrum was determined. In addition, the effect of quantum wire diameter variation on absorption was evaluated.

To guide the nanostructure array development effort, an engineering model was developed to determine the primary absorption features of $Cd_{1-x}Zn_xS$:Cu quantum wires as a function of alloy composition and diameter [149]. It is generally accepted that in this material system the metal impurity center (Cu) behaves as an acceptor for deep level energy transitions between this state and the conduction band [150, 151]. The ionization energy of the excited Cu acceptor sub-levels used in these calculations is based on those measured by Heitz [151] for low dopant levels ($< 10^{18}$). All other experimental values were obtained from Landolt-Bornstein [152].

The calculations presented below are based on the one electron model for the acceptor energy levels. This model assumes the following relationship for the band-gap due to quantum confinement in a

parabolic potential. The ionization potentials for the acceptor and donor levels are assumed constant relative to the top of the valance band (VB) and bottom of the conduction band (CB) respectively. Under quantum confinement, the CB and VB correspond to the n=0 states for the discrete conduction and valence energy levels. All ionization levels are measured relative to these discrete levels in the forbidden region. All properties based upon compositional variation in ZnCdS:Cu are presently assumed as a linear interpolation as a function of x. The results of this analysis are shown in Figure 5-2 with the absorption wavelength as a function of alloy composition and quantum wire diameter.

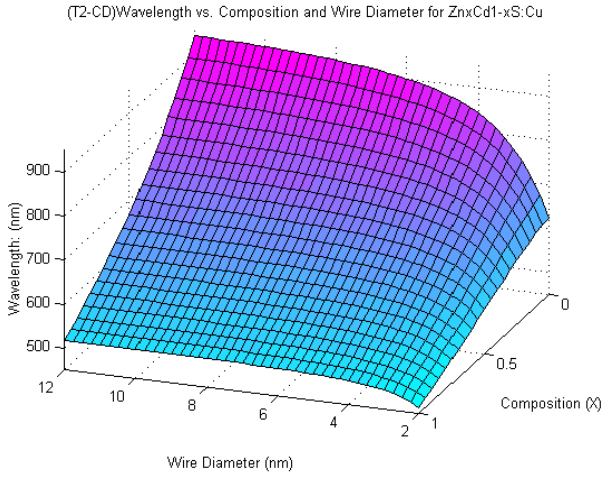

Figure 5-2 Peak absorption wavelength of ZnCdS quantum wires as functions of wire diameter and alloy composition.

A more sophisticated analysis was employed in collaboration with Daniel Gray to determine the effect of a distribution in quantum wire diameter on the absorption properties of the nanostructure arrays [149]. This analysis is based on a shooting-technique solution of the Schrodinger equation as presented by Harrison [153]. The variation in quantum wire diameter was taken to follow a

Gaussian distribution around a mean diameter of 8 nm. The energy of the lowest energy transition was then calculated for each diameter of wire and weighted by the number of wires with that size in the distribution. The results of this analysis are shown in Figure 5-3. The resulting absorption energies match the theoretical and experimental results reported by Kayanuma [154]. There are two primary features to note from these results. First, although the distribution of quantum wire diameters is assumed to be Gaussian, the resulting distribution deviates from this due to the non-linear relationship between nanostructure size and absorption energy. Second, a fairly narrow peak is seen for a distribution of 5% in nanostructure diameter. This spread is not seen to rapidly increase until a variation of 20% is seen. This is significant since our variation in pore size is expected to be less than 5%, especially for multi-layer anodization.

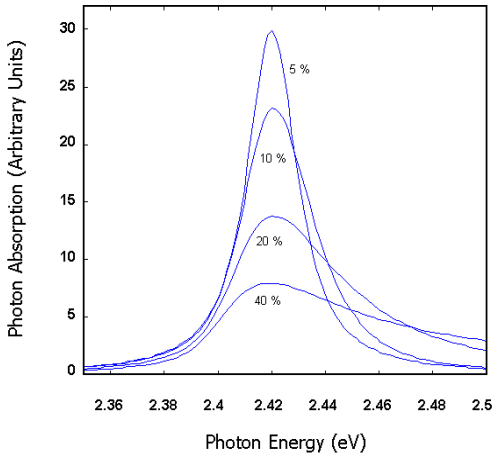

Figure 5-3 Effect of size distribution on the absorption spectra of CdS quantum wires. Mean wire diameter : 8 nm.

Finally, a complete absorption spectrum was calculated for a CdS quantum wire diameter of 8 nm in collaboration with Daniel Gray. The results are displayed superimposed on the solar spectrum both at the earth's surface and at the top of the atmosphere (Figure 5-4). This shows that the absorption peaks for a single layer nanostructure coincide relatively well with the peak intensity of the solar spectrum.

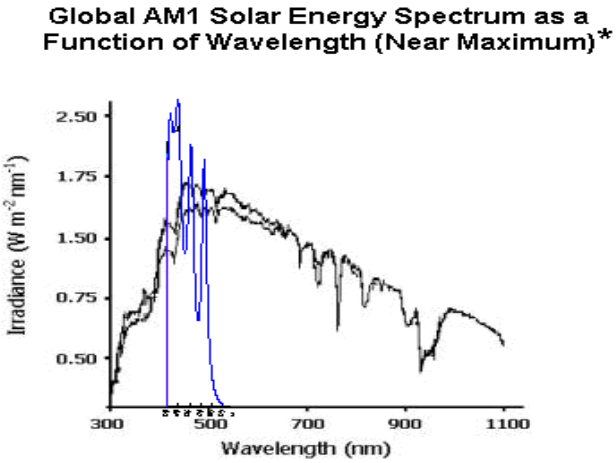

Figure 5-4 Absorption spectra of 8 nm diameter CdS quantum wires superimposed on solar spectra

5.2 Silicon Surface Texturing

Surface texturing is commonly used in crystalline silicon photovoltaic cells to improve light absorption and therefore enhance total cell efficiency. In this approach, multiple reflections off of the textured silicon surfaces increase the probability of photon absorption in the active silicon material. When combined with suitable anti-reflection coating, this approach has been demonstrated to significantly enhance the efficiency of crystalline silicon photovoltaic cells [155, 156]. Techniques for surface texturing for both mono- and poly-crystalline silicon have been an active area of research. For the case of mono-crystalline silicon, the use of an anisotropic etch that is selective to crystal orientation is commonly used. This approach has evolved from the use of etched square-based pyramid structures in the early COMSAT cells [157], to the inverted pyramid structure used in the high efficiency PERL cells [158]. In addition, lithographic processes have been developed for surface texturing in high efficiency mono-crystalline PV cells [155]. For the case of poly-crystalline silicon devices, anisotropic etch techniques are not appropriate due to the lack of well defined crystal planes. The use of random texturing has been developed for multi-crystalline

silicon, however a large percentage (28 %) of the incident light is reflected from these randomly textured surfaces [159].

Several different approaches have been previously investigated to provide surface texturing for poly-crystalline silicon. These include mechanical grooving [160], defect etching with acidic solutions [161], reactive ion etching (RIE) [162], and lithographic surface patterning [146, 163]. This combination of isotropic etching through apertures defined with photolithography has been used to demonstrate a "honeycombed" textured surface that led to a 19.8% efficient poly-crystalline silicon PV cell [163]. In addition, the same honeycombed structure was used to demonstrate a 24.4% efficient mono-crystalline silicon PV cell [146]. However, these techniques present several problems for commercial device applications. While considerable work has been done on mechanical grooving, low-cost metallization on the deeply grooved surfaces is difficult. Defect etching requires the use of a large amount of proprietary acidic solutions. RIE is a relatively slow vacuum process that can also induce unwanted damage to the silicon surface. Finally, the use of lithographic processes for texturing is not cost-effective due to equipment expense and low throughput. As a result, it is important to develop a low cost, manufacturable surface texturing technique that can provide control over pore shape and dimension, and is applicable for both mono- and poly- crystalline silicon. To meet this challenge, a method of non-lithographically creating a subwavelength structured surface was developed as shown in Figure 5-5.

5.2.1 Subwavelength Structured Surfaces

Subwavelength structured (SWS) surfaces are composed of regular arrays of small structures with a wavelength smaller than that of the incident electromagnetic radiation [164]. Although originally developed for microwave engineering, this phenomena was applied to optical wavelengths by

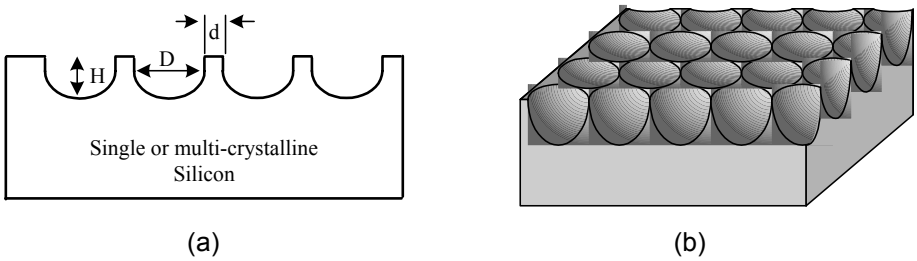

Figure 5-5 Subwavelength surface texturing of silicon solar cells : (a) cross-sectional and (b) perspective views.

Bernhard who correlated features on the corneas of moths with the reduced reflection from their eyes needed for night camouflage [165]. Experimental results indicate that SWS surfaces can substantially reduce reflection from semiconductor materials by up to two orders of magnitude in both the visible and infrared regions [164, 166]. Theoretical calculations using the rigorous coupled-wave analysis (RCWA) show that for silicon, optimum anti-reflection properties are obtained for a 2-dimensional SWS surface with feature periodicity of 100 nm [166, 167]. For this structure, these calculations show that reflection at 600 nm decreases from 35% to approximately 0.5%. These results were verified experimentally using structures defined using holographic recorded cross gratings and formed by Reactive Ion Etching [164]. Very recently, similar structures were formed using an alumina template mask formed on a bulk aluminum substrate, removed by an $HgCl_2$ etch, and affixed to a silicon substrate by drying [167]. SWS features were then formed in the silicon substrate by etching with an SF_6 fast atom beam. The experimental reflectivity data matches that of Lalanne [164] and is consistent with the RCWA calculations.

5.2.2 Fabrication

The texturing will be accomplished by electrochemically etching the silicon substrate through the pores in the anodized alumina template. Electrochemical etching or electropolishing of silicon is a

well investigated and established process [168] and is performed in a solution of HF and H_2O_2 with current densities of 100 mA/cm^2 and above. It should be pointed out that porous silicon is fabricated by a similar technique and in a similar electrolyte, however at lower current densities. While porous silicon forms nanometer scale silicon structures, electropolishing completely etches the silicon material in a defined area. It is also emphasized here that the electropolishing technique is equally appropriate for both mono- and multi- crystalline silicon; the anodization technique has been successfully used to fabricate porous silicon on poly-crystalline silicon as well [169].

The process flow for surface texturing of mono- and poly- crystalline silicon is summarized in Figure 5-6. The silicon substrate is coated with a thin layer of aluminum by sputter deposition. The aluminum layer is then anodized in H_2SO_4 using the appropriate current density. The process will be monitored by observing voltage-time characteristics to make sure the pores contact the silicon substrate. A pore widening process in H_3PO_4 will be carried out, if necessary, to reduce the inter-pore spacing. The silicon substrate will then be electropolished through the alumina template in a solution of HF and H_2O_2 at the appropriate current density. The alumina template will then be removed by dissolving it in a solution of NaOH.

5.3 Summary

The application of non-lithographic fabrication technology to the formation of nanostructure-based photovoltaic devices is particularly appropriate due to the requirements for commercial device applications. In particular, non-cryogenic operation requires the fabrication of structures with characteristic dimensions less than 20 nm. However, photovoltaic device operation requires the fabrication of devices with active areas on the order of several meter^2. The contrast between these two length scales makes fabrication of nanostructure-based photovoltaic devices nearly impossible

using conventional lithographic techniques. As a result, electrochemical based synthesis techniques as described in this chapter are particularly appropriate due to the ability to fabricate devices across length scales in an economical matter. For this reason, it appears that photovoltaic devices are perhaps the most important market for this technology.

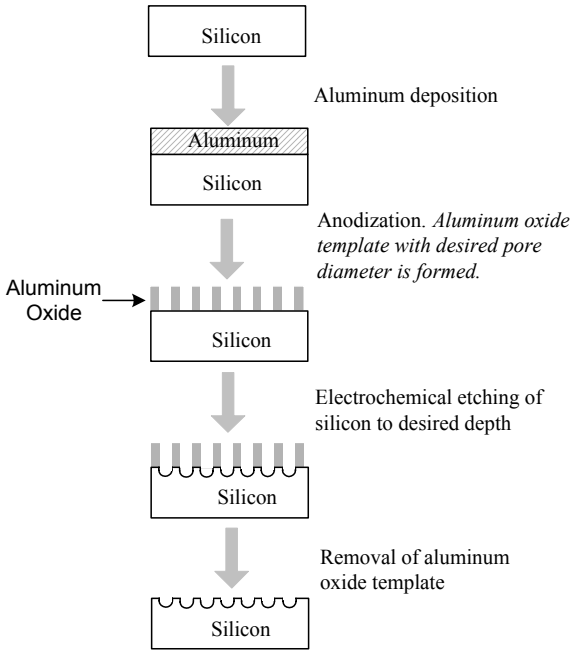

Figure 5-6 Process-flow for surface texturing of mono- and poly- crystalline silicon

Chapter 6

Conclusions and Future Work

The primary goal of this research has been to develop a fabrication process for the synthesis of semiconductor nanostructure devices on an arbitrary substrate material. This is enabled through the creation of a template containing an ordered array of nanoscale pores. In particular, the development of the Al/Pt/Si structure with *in situ* barrier layer removal allows the direct DC electrochemical synthesis of semiconductor nanostructures with increased crystalline order.

This work has demonstrated that the use of an alumina template based synthesis technique is a viable fabrication option for the development of nanostructure-based photonic devices. In particular, this technique is particularly well suited for the development of photovoltaic devices and silicon based photonic devices. For photovoltaic devices this is due to the scalability of the fabrication technique and the ability to fabricate structures on different length scales. In the case of silicon devices, this approach enables direct integration of nanostructures with silicon CMOS technology.

In addition to direct material synthesis inside the template pores, it has been demonstrated that the alumina template can be used as a mask for the etching of nanoscale structures on a silicon substrate. This was demonstrated for both plasma based etch techniques (RIE), and electrochemical anodization (porous silicon formation). The ability to fabricate porous silicon through an alumina

template enables a potential mechanism to address the issue of material reliabiltiy by the formation of a hydrated alumina protective coating.

The future work in this area can be divided into three categories: materials synthesis and characterization, pattern transfer development, and device development. Materials synthesis work will concentrate on the development of an underpotential-DC electrochemical technique for the synthesis of semiconductor nanostructures with atomic layer precision. Preliminary analysis indicates this technique can be used for the fabrication of semiconductor heterojunctions (i.e. CdS/CdTe). The material synthesized will be characterized by photoluminescence, Raman, FESEM, and HRTEM imaging. The pattern transfer technique will be investigated through the use development of an appropriate RIE etch process to provide both anisotropy and sidewall passivation. In addition, the use of electrochemical etch techniques will be investigated for subwavelength surface texturing of crystalline silicon nanostructures. Finally, device design will concentrate on the development of reliable contacts to the semiconductor nanostructures, as well as the development of models for optical processes and carrier transport within the semiconductor nanostructures.

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Appendix A

The Effect of an Applied Electric Field on the Optical Properties of Porous Silicon

If the quantum size effect is responsible for the visible light emission in porous silicon, the photoluminescence and the optical absorption properties of the material are expected to be altered by the presence of an applied electric field through the quantum confined Stark effect (QCSE). QCSE is a well known phenomenon observed in semiconductor low dimensional structures, where excitonic effects dominate optical properties . In such systems, when an electric field is applied parallel to the direction of quantum confinement, a red-shift is observed in the photoluminescence spectra together with a reduction in the PL intensity. However, when the electric field is applied perpendicular to the quantum confinement direction, no such red-shift is observed. The absorption spectra of the material also exhibits a similar behavior, showing a red-shift of the absorption edge together with an increase in the absorption coefficient when an electric field is applied parallel to the direction of quantum confinement. Since QCSE is quantum mechanical in origin, the optical property modulation caused by it is extremely fast, and a number of high speed optoelectronic devices has been proposed based on this effect [1]. If quantum confinement plays an important role in porous silicon, it is plausible that its optical properties can be modulated through the quantum confined Stark effect thus raising the possibilities of high speed electro-optic device applications of this material.

To investigate the effect of electric field on the photoluminescence spectra, two different device structures were fabricated. Cross-sectional diagrams of the two devices, referred to as the *perpendicular field device* and the *parallel field device* are shown in Figures 1(a) and 1(b) respectively. The device labels indicate the direction of the applied electric field relative to the porous silicon growth direction. For both devices, the starting wafers were p-type {111} 0.1-0.3 Ohm-cm single crystal silicon wafers. Prior to anodization, the back of the wafers were coated with aluminum followed by an annealing step to provide good back ohmic contact. The wafers were then anodized in 49% HF and ethanol solution. For the perpendicular field device, the anodization was carried out for 10 minutes.

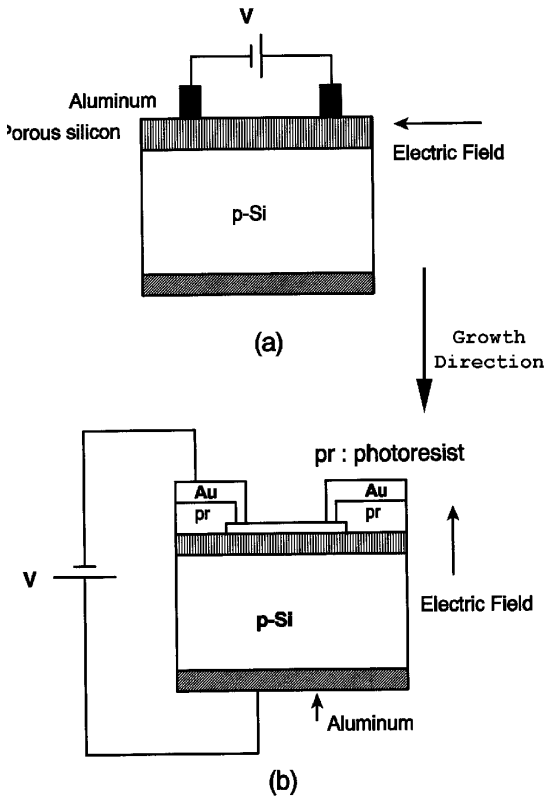

Figure 1:Cross sectional structure of (a) the perpendicular field device and (b) the parallel field device. The device labels indicate the direction of the applied electric field relative to the porous silicon growth direction.

After anodization, aluminum metal lines with 2 mm spacings were deposited on the porous silicon surface through a shadow mask to form the electrodes for application of the electric field. There was no annealing performed on the top aluminum electrodes. For the parallel field device, anodization was performed at a fixed current density of 50 mA/cm^2 for only 30 seconds to keep the thickness of the porous silicon layer small (~1 micron) in order to produce sufficiently large electric fields. Immediately after anodization, a pre-oxidation step was performed on the porous silicon layer for 1 hour at 300^o C to form a thin layer of oxide on the surface. Next, a thin film of gold (~ 10 nm) was deposited on the surface of the porous silicon to form a semitransparent electrode. The gold electrode was contacted using a 300 nm thick gold layer for external connections. Since similar anodization parameters were used for the perpendicular and the parallel field devices, their porosities and optical characteristics are also expected to be alike.

Photoluminescence measurements were performed on the perpendicular and the parallel field device at different electric fields. The PL spectra were measured at 12K using an Ar^+ ion laser, a one meter single pass monochromator, photomultiplier tube and standard photon counting electronics. The laser beam was focused in the inner-electrode gap for the perpendicular field device, and on the thin semi-transparent gold electrode for the parallel field device. The effect of perpendicular electric fields on the photoluminescence spectra is presented in Figure 2 where the spectra for only three different voltages are shown for clarity. Without any electric field present, the PL spectrum shows a peak energy of 1.73 eV which corresponds to a blue-shift of 0.63 eV from crystalline silicon. With increasing electric fields, the photoluminescence spectra show clear red-shift together with quenching of the PL intensity. For an applied voltage of 120 V across the aluminum electrodes (spacing of 2 mm), the red-shift observed was 65 meV with an almost 50% reduction in the PL intensity. The positions of the PL peak energies as a function of the applied voltage is shown in Figure 3. Similar photoluminescence quenching with electric field has been also observed by Lue

et. al.[2], however they did not report any red-shift in the PL peak intensity; the absence of a red shift may be due to the low value of electric field (29 V/cm) used in their experiments.

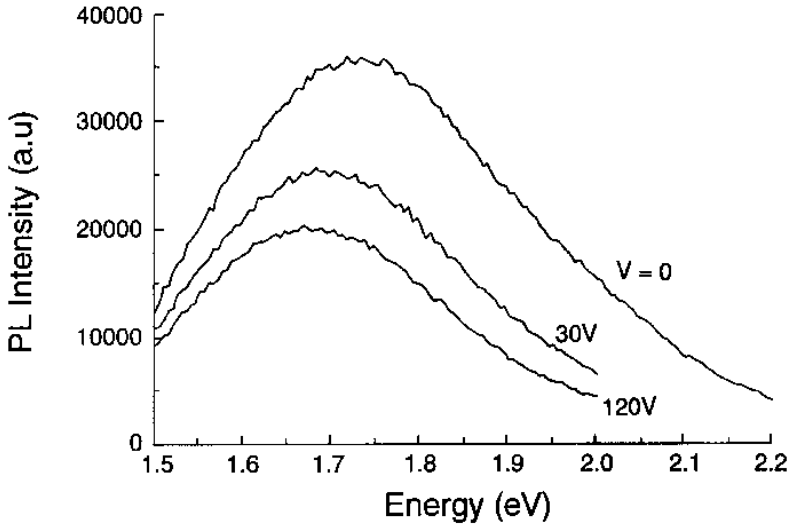

Figure 2: The photoluminescence spectra of porous silicon under an electric field applied perpendicular to the porous silicon growth direction.

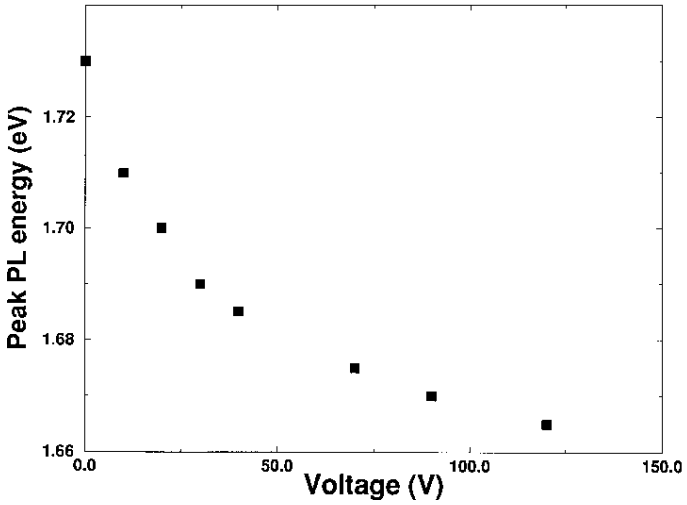

Figure 3: The dependence of the photoluminescence peak energy position on the applied voltage for the perpendicular field device.

The effect of electric field on the photoluminescence spectra for the parallel field device is shown in Figure 4. The PL intensity measured in these devices was much weaker due to attenuation of light in the semi-transparent gold electrode. From Figure 7, the peak PL energy for the parallel feild device is approximately at 1.74 eV which is very similar to that observed for the perpendicular field device. Such similarity is expected due to the similar anodization parameters used in the two types of devices. The data in Figure 4 is some what noisy, however, the PL spectra do not show any clear evidence of red shift, although the PL intensity is reduced with increased electric fields. The data observed in Figure 4 is qualitatively similar to the quenching of PL intensity observed by Koyama [3]and Parkinson [4] with an electric field applied parallel to porous silicon growth direction.

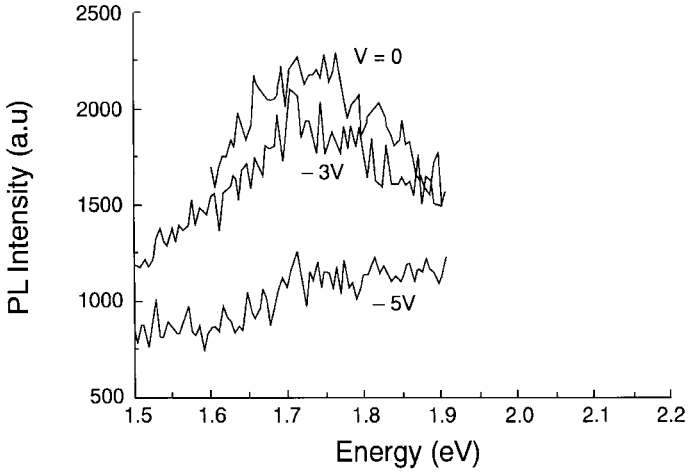

Figure 4: The photoluminescence spectra of porous silicon under an electric field parallel to the porous silicon growth direction.

Based on the above results, we next investigated the effect of an electric field on the optical absorption properties of porous silicon. Since crystalline silicon has a lower band-gap compared to porous silicon, it is not possible to perform transmission measurements with the substrate present. Usually, this is circumvented by separating the porous silicon from the substrate through electro-polishing. However, we found that self-supporting PS structures created by anodizing completely through a thinned layer of silicon provide better stability and handling. The starting material for this device was p-type {111}, 0.1-0.3 Ohm-cm substrate with a thickness of 375 microns. The wafer was masked and patterned, and a circular area was etched down to 200 microns using a (1:4:1) solution of $HF:HNO_3:CH_2COOH$. The sample was then anodized completely through the 200 micron thick central layer resulting in a porous silicon structure that could mechanically support itself due to its large thickness. Next, two 500 nm thick aluminum pads with a spacing of 1 mm were deposited on top of the PS film for the application of an electric field perpendicular to the porous silicon growth direction. The absorption spectra were then measured using a Perkin-Elmer Lambda Array 3840 UV/Visible Spectrophotometer at 12 K, and the results are shown in Figure 14. The figure shows that with increased electric field, the absorption spectra is broadened and the absorption edge undergoes a red-shift accompanied with an increase in the absorption coefficient.

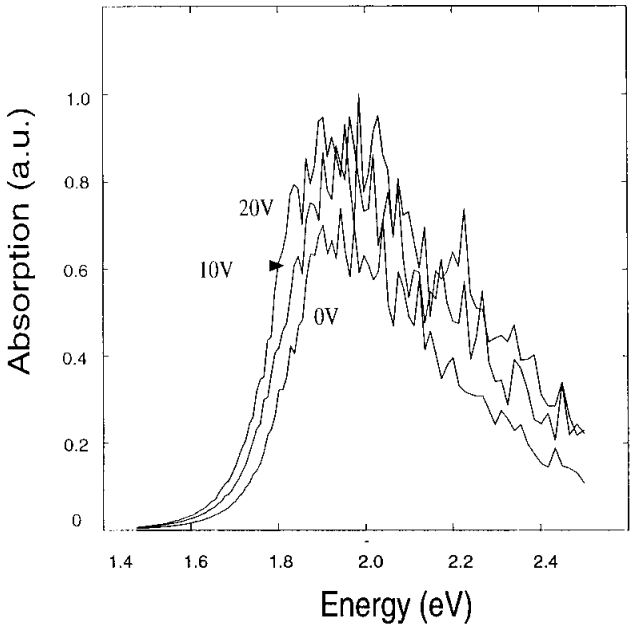

Figure 5: The absorption spectra of the self supporting porous silicon film under an electric field applied perpendicular to the porous silicon growth direction.

The experimental data presented above show strong resemblance to the quantum confined Stark effect (QCSE) described earlier. Both the photoluminescence and the absorption spectra show a red-shift with increasing electric field. Also, the photoluminescence intensity was reduced and the absorption coefficient increased with increasing electric field as is expected for QCSE. After a detailed analysis of the experimental data, we conclude that direct quantitative correlation with theoretical predictions are not possible due to the non-uniformity of the internal electric field in porous silicon[2]. However, based on our analysis presented below, it does seem reasonable to attribute the experimental results at least partially to QCSE.

Without an applied electric field, the PL spectra show a peak at 1.73 eV (Figures 11 and 13) which closely matches the absorption edge (Figure 14). This indicates a blue-shift of 0.63 eV compared

to the band-gap of crystalline silicon. Using the quantum confinement model, this blue-shift implies that the PS layer is composed of nanostructures with a diameter of 3 nm. However, it is important to note that porous silicon is a highly non-uniform material, and the 3 nm estimated diameter refers to the dominant structure that contributes to the optical absorption and photoluminescence characteristics of the material. Although it is difficult to determine the exact magnitude of the electric field inside the PS film, the potential drop across a quantum confined structure needed to produce the observed red-shifts can be estimated from electrostatic considerations. The largest red-shift observed in the PS spectra is 65 mV, which corresponds to an internal electric field of $2x10^7$ V/m. This is less than the breakdown field of silicon ($3x10^7$ V/m), and electric fields of this magnitude have been previously reported in porous silicon[5]. Also, for QCSE observed in two dimensional structures, such as quantum wells, the red-shift shows a quadratic dependence on the electric field [1]. The data in our devices (Figure 3) do not show such a quadratic dependence and instead could be best fitted by a third order polynomial. This is consistent with a theoretical investigation of the properties of CdS nanostructures which shows a higher order dependence of the red-shift on applied electric field [6], claimed to be due to the modification of the exciton binding energy caused by the applied electric field.

In summary, we have experimentally demonstrated a red-shift in PL peak position and quenching of the PL intensity with an electric field applied perpendicular to the porous silicon growth direction. We have also demonstrated a similar behavior in the electro-absorption characteristics of a self-supporting porous silicon film. These results agree qualitatively with the quantum confined Stark effect that is commonly observed in low dimensional semiconductor structures. Besides providing additional indications that the optical properties of PS are possibly due to the result of quantum size effect, the experimental electro-absorption data also demonstrates the potential of this material for silicon based electro-optic devices.

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Appendix B

Pulsed Current Anodization of Porous Silicon

The interest in porous silicon (PS) is fueled by its potential applications in silicon based optoelectronic circuits[1, 2]. The recent demonstration of a porous silicon light emitting device modulated at 200 MHZ [3], and the implementation of a PS based optoelectronic circuit [4], indicate the real possibility of this material for practical applications. Optoelectronic applications, however, will require efficient PS based light sources that are both reliable and reproducible, and a PS based PN junction light emitting diode (LED) is appropriate and a realistic objective. A number of different porous silicon LEDs have been already demonstrated [5-12], however, significant improvements in device fabrication, performance, and stability are still required before any practical applications of such devices become possible.

The investigation of porous silicon PN junction LEDs has been confined primarily to unpatterned structures where the PN junction is formed through out the whole wafer using blanket doping . The area of such an LED is primarily defined by the top electrode. Although such devices are useful for demonstration purposes, patterned LEDs with lithographically defined features are preferred for their compatibility with crystalline silicon manufacturing process, and their improved reliability and performance[2]. In addition, the P and N regions of the LEDs are desired to be heavily doped since higher doping leads to improved device performance through (i) increased majority carrier injection in LEDs, (ii) reduced LED threshold voltage, and (iii) increased light emission efficiency. However, as described below, anodization of patterned PN junctions using DC currents was found to be very

difficult, and in case of heavily doped structures almost impossible. To eliminate this problem we have investigated and developed a pulsed current anodization method where current pulses are used to anodize the heavily doped patterned PN junctions.

PN junction structures were fabricated on P-type {111} crystalline silicon substrates of 0.1-0.3 Ω-cm resistivity. A number of PN junctions, approximately 1.5-1.7 μm deep, were formed by diffusion of N-type impurity through an oxide mask with the N-regions approximately 2 mm in diameter. Next, an aluminum layer was evaporated on the back of the substrate and annealed to form an ohmic contact to facilitate anodization and testing. The electrolyte used for anodization was 2:1:1 mixture of ethanol, HF and H_2O. After anodization, the wafer was rinsed in deionized water and dried naturally in air. The samples were then immediately loaded in a vacuum chamber and a 12 nm thick layer of gold, 1.5 mm in diameter, was deposited on top of the N-layer through a shadow mask to serve as the semi-transparent top electrode.

Initially we attempted to anodize the PN junction structures using a constant DC current. It was found that the P-region alone was being anodized and the N-region remained relatively unaffected. If the anodization was carried out for a long period of time, the N-layer could be partially anodized, but it was not possible to anodize through the full thickness of the N-layer even with extended anodization periods. We believe that this is caused by preferential current flow in the P-type material due to the configuration of the top electrode and the potential barrier at the PN junction.

During anodization, the electrolyte serves as the top electrode which contacts the whole surface of the wafer, both the p and the n-regions (Figure1a). For the N-layer to be anodized, it is necessary for the anodization current to flow across the PN junction into the N-layer. However, due to the potential barrier at the junction, the anodization current initially flows only through the low

resistance P-layer that surrounds the N-region. As a result of this preferential current flow, the P-type material surrounding the N-layer becomes anodized, leaving the N-layer relatively unaffected. However, as the P-layer becomes more porous, its resistance increases, and a portion of the anodization current begins to flow across the junction into the N-layer. This is why, when the anodization was carried out for a long period of time, it was possible to partially anodize the N-layer.

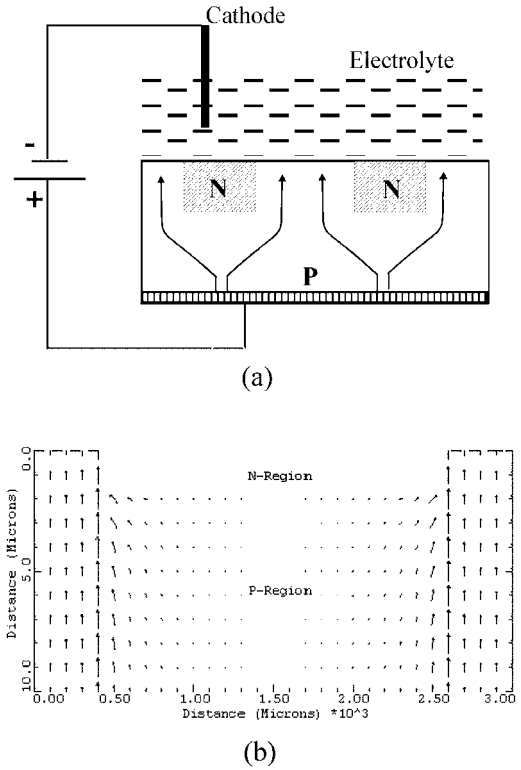

Figure 1: Current distribution during anodization in patterned PN junction structures a (a) predicted, and (b) simulated.

This explanation was confirmed by a simulation of the PN junction structure using the MEDICI electrostatic device simulation program provided by Avanti corporation. MEDICI self-consistently solves the Poisson equation and the carrier continuity equation on a two-dimensional grid. The simulated device was designed to match the doping density and dimensions of the experimental

devices. The current flow through the device was determined by a two-carrier solution using the concentration and field dependent mobility models. The results of this simulation are shown in Figure 1b with the vectors indicating the direction of current flow at each grid point. The length of the vector is directly proportional to the magnitude of the current flow at each grid point.

From the simulations it is seen that the current flowing in the N-layer is only a small part of the total anodization current. This implies a very low anodization rate in the N-layer. This problem is significantly increased for N-layers that are heavily doped since the anodization rate of N-type silicon decreases with increased doping density.

It was also observed that anodization performed under ultra-violet (UV) light did not increase the anodization rate of the N-layer. UV light is typically used during anodization of N-type materials to provide the positively charged holes that are necessary for the electro-chemical reactions to take place. We believe that when anodization of the N-layer begins, holes are injected across the PN junction and into the P-layer, and are therefore not available for the electrochemical reaction. This would explain why UV illumination does not increase the anodization rate of the N-layer.

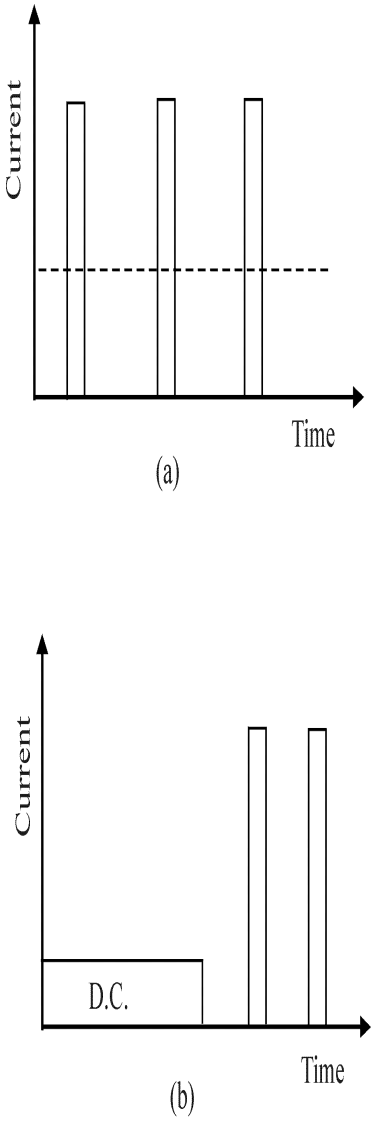

Figure 2: Current profiles for (a) pulsed current anodization, and (b) DC + pulsed current anodization. The dashed line in (a) indicates the threshold current for electropolishing

A possible solution to the problem of anodizing heavily doped PN junctions is to substantially increase the anodization current which would increase the anodization rate in the N-layer. However, there is a limit on the maximum anodization current that can be used, after which electropolishing takes place and damages the device. To circumvent this problem, we have developed the technique of pulsed current anodization of porous silicon [13] (also reported in [14] later on). Using this method, a sequence of current pulses are used to anodize the heavily doped structures (Figure 2a). This allows the use of a large current density to increase the anodization rate in the N-layer, without the risk of electropolishing the LED structures.

We have fabricated a number of porous silicon PN junction LEDs using the pulsed current anodization technique. PL measurements confirmed (described below) that the n layers were completely anodized without peel-off or electropolishing. We have also developed a combination

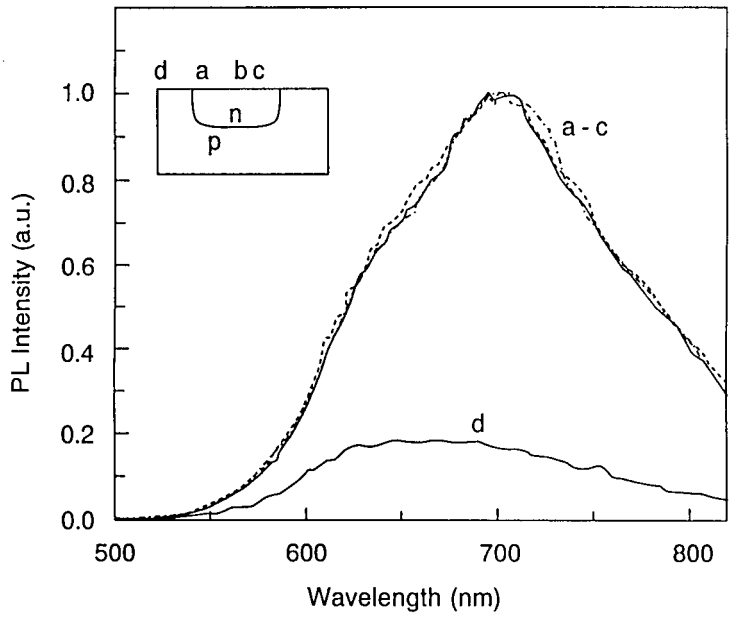

Figure 3: Photoluminescence spectra at various points on a patterned PN junction structure anodized with pulsed current.

of pulsed and DC currents during anodization which appear to produce better results (Figure 2b). A constant DC current is first used to anodize the surface of the P-layer surrounding the N-region. Since the porous P-layer has a large resistance, the percentage of anodization current flowing through the junction was increased during the application of the pulsed currents.

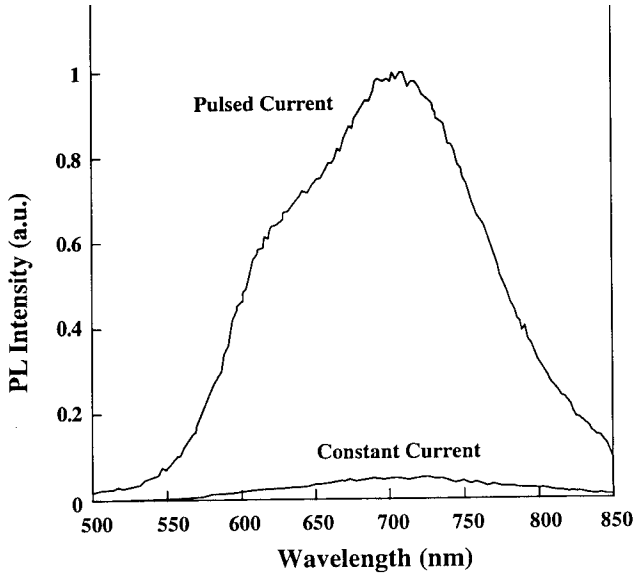

Figure 4: Comparison of photoluminescence spectra for devices anodized with pulsed current and direct current.

A patterned porous` silicon PN junction LED fabricated by the pulsed current anodization method was performed by a constant DC current (l0mA/cm^2) for 30s followed by a sequence of 10 pulses of 5s duration at 370mA/cm^2 current density. Figure3 shows the PL spectra from different points on the device. All PL spectra were measured by direct excitation of the porous silicon surface using the 364nm line from an Argon ion laser. The upper three spectra were obtained from different points on the PN junction area (points a, b and c) to check the surface uniformity, which, from Figure 3, was found to be excellent. The lower spectrum was obtained from the P-type porous silicon surface outside the patterned area (point d). From Figure 3, the PL spectrum from p type porous silicon has

a peak wavelength of around 650nm while the PL spectra from the porous silicon PN junction have two peaks at 700nm and 650nm. This suggests that the PL from the junction area is composed of light emission from both N-type and P-type porous layers, confirming the formation of porous silicon all through the PN junction.

Figure 4 compares the PL spectra from a pulsed current anodized device with that from a constant current anodized device (50mA/cm^2 for 5 minutes). Both spectra have a peak at 700nm which indicate that the N-region in both devices have the same porosity. However, the PL intensity for the pulsed current anodized device is more than an order of magnitude higher than that for the constant current anodized device, indicating that the N-porous layer is thicker for the pulse-current anodized device.

Some preliminary results on LED characteristics fabricated by the pulsed current anodization are presented below. Detailed results of measurement together with comparisons of DC anodized and pulsed current anodized LEDs will be presented elsewhere[15]. The LED has a non-ideality factor of 5.74 and a series resistance of 241Ω. All LEDs fabricated by the pulsed current anodization technique emitted visible light under forward bias condition; visible light was observed to emit uniformly from the PN junction area and the light intensity increased linearly with the forward bias current. This was in direct contrast to the DC current anodized LEDs which showed light emission only under reverse bias conditions.

As discussed previously, a heavily doped PN junction is desired for the fabrication of porous silicon LEDs. To investigate the effect of doping density on LED performance, we have fabricated devices with two different doping densities. For device-l, the doping density in the p and n regions were 2xl0^{17}/cm^3 and 5xl0^{19}/cm^3 respectively, whereas for device-2, the p and n doping densities were

$8xl0^{19}/cm^3$ and 1.5 X 10^{20} / cm^3 , respectively, as shown in Table I. Porous PN junctions were fabricated using the pulsed current anodization technique discussed previously. Both devices showed electroluminescence under forward bias condition. The threshold voltage and current for light emission are shown in Table 1. From Table I, it can be seen that the threshold voltage of porous silicon LEDs can be lowered significantly by increasing the doping density in the junction area, an important factor for practical applications of these devices. An area of concern for porous PN junction LEDs is their lifetime, which in our case ranged from several minutes to several hours. The failure mechanisms for these devices are not clear at this time, and are currently under investigation. Also, the quantum efficiencies of these devices, for which we do not have any quantitative data at this time, appear to be quite low. We believe that the quantum efficiency can be improved by optimizing the device design and fabrication, such as substrate resistivity, doping density, junction depth and anodization conditions, and is currently under investigation.

Table I. LED threshold voltages and currents for devices with different doping densities.

Device	Doping densities / cm^3	Threshold voltage & current
1	$N_A = 2x1^{17}$, $N_D = 5x1^{19}$	42 V, 6 mA
2	$N_A = 8x1^{19}$, $N_D = 1.5x1^{20}$	5 V, 20 mA

In summary, we have successfully fabricated porous silicon PN junction LEDs from heavily doped patterned PN junctions. The traditional DC current anodization was found to be unsuitable for the anodization of these structures. Successful anodizations were performed by using pulsed currents, where large current densities can be used with out the risk of electropolishing. Photolumiscence measurements performed on these devices confirmed that the N layers were anodized completely through the PN junctions. The LEDs show uniform visible electroluminescence under forward bias conditions. In addition, the investigation of the effect of doping density on device performance shows that the LED threshold voltage can be lowered by increasing the doping density in the device.

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