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Analog Intelligent Wake-Up Systems for Wireless Sensor Networks

by

Robert Joseph Fernandez

Thesis submitted to the
College of Engineering and Mineral Resources
at West Virginia University
in partial fulfillment of the requirements
for the degree of

Master of Science
in
Electrical Engineering

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2011

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Wake-Up, Vision System, Sub-threshold, Analog, CMOS

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Abstract

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The applications of Wireless Sensor Networks have grown exponentially over the last several years. These networks help to monitor environmental parameters such as temperature, humidity, pollution, motion, acoustics, and vibration in a variety of different ways. Each node (mote) in the network typically contains the following: a microprocessor, sensors, circuits that interface sensors with the mote, a radio transceiver, and a power source; typically a battery.

These sensor networks typically work by having the mote's Analog-to-Digital Converter (ADC) convert raw analog sensor data into digital, so processing can be done by the mote's microprocessor. If an event of interest has occurred, the mote transmits relevant data using its radio. However, if the data being read by the sensors are not of interest, the power consumed by the processor and ADC is wasted. This valuable energy is being used because of the mote's need to operate off of battery power.

Presented in this work are several analog systems with the ability to use Analog Signal Processing (ASP) prior to sending an interrupt to a higher level system. The first system is modeled on work previously conducted by Brandon Rumberg, and is used as a spectral analysis wake-up system. This system is used to detect programmable frequency content. If the content matches a predetermined template, an interrupt is given and the mote is awakened from its sleep state. The second system discussed is a biologically inspired vision system. This system uses ASP to detect objects moving. If the object is moving in a programmable speed range, an interrupt is given and the mote will awaken from its sleep state. The third system is a redesigned version of the biologically inspired vision system. The new system detects motion similarly to the previous system, however it has the ability to detect object speed as well as direction.

The ability to use ASP to pre-process the event before mote wake-up makes these two systems extremely important. By doing such, energy is saved and higher level processing is still possible once the information is converted into its digital form by the mote.

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Chapter 1

Introduction

The applications for wireless sensor networks (WSN) has grown in use exponentially over the past several years. Examples include habitat and environmental monitoring, calamity detection, traffic control, remote health care and many others [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12]. Each wireless sensor node typically contains a radio transceiver, sensor(s), microcontroller, circuit(s) which interface with the sensor(s), and an energy source typically a battery. Each WSN node (mote), typically uses its Analog-to-Digital Converter (ADC) to read data from an analog sensor at a desired frequency prior to determining if the event or the signal data is of interest or not. Present-day sensor interfacing is inadequate for these types of low-power systems because of high power consumption and data storage.

Fortunately, sub-threshold circuits provide a low power alternative to digital sensor networks. By using sub-threshold analog circuits, data can be extracted from the real world continuously, while the mote remains in its low-power sleep state. Instead of sending an interrupt to the mote directly, the data can be processed using an Analog Signal Processor (ASP). By using an ASP, the mote's processor is freed from processing these interrupts, while maintaining the ability to process information further after data is converted using the ADC.

The objective of this work is to develop low-power wake-up systems by using

several alternative analog based systems. These systems use ASP to detect events and wake-up a higher level system only when an event of interest has occurred. The first system is an analog-based spectral analysis system for use as a frequency detector. The second system is a biologically inspired vision system for use as a motion detector. These two separate systems contain sensors which interface with the natural analog signals, and then interpret the information received before a digital system processes the information. A new velocity detection system capable of detecting object velocity as well as direction is also discussed. This new system is capable of being used in conjunction with the biological vision system, and can also be used independently to cause its own system wake-up.

1.1 Analog Over Digital

The Webster's dictionary defines analog as "a mechanism in which data is represented by continuously variable physical quantities". Digital devices are devices which round these continuous signals to form a series of ones and zeros. A simple example to distinguish the difference between analog and digital is to compare two clocks. An analog clock is able to represent all times through a day, while a digital clock is capable of representing only finite differences in time, such as every tenth of a second. The world in which humans live is an analog world. The sounds and sights we see and hear are all analog signals; each having continuous values which are interpreted in different ways. Since analog sensors interact with our analog world, using analog circuitry to operate on the analog data only makes sense. Converting from an analog domain to a digital domain can be avoided by using analog circuits to interface with the analog data. This modification saves power by avoiding the use of the ADC and the microprocessor. Some common analog circuits include filters and amplifiers. Sub-threshold operating points of these analog circuits can be used to provide the type of low-power alternative capable of creating entire systems which

consume less than $1\mu\text{A}$.

1.1.1 Sub-Threshold Analog Circuits

Complementary Metal Oxide Semiconductors (CMOS) are used quite frequently for digital circuits. By combining analog and digital systems using the CMOS process costs can be cut and device sizes minimized. Since several type of sensors can be created in a CMOS process, this becomes beneficial for our current application.

Low-power CMOS circuits are achieved by biasing the transistors in weak-inversion, or sub-threshold region. In sub-threshold the current through an n-channel Metal Oxid Semiconductor Field Effect Transistor (MOSFET) is described by

$$I = I_0 e^{\frac{\kappa V_g}{U_T}} \left(e^{\frac{-V_d}{U_T}} - e^{\frac{-V_{d'}}{U_T}} \right) \quad (1.1)$$

where κ is the slope factor, U_T is the thermal voltage ($\approx 26 \text{ mV}$), and I_0 is dependent on transistor sizes and process constants.

Transistors operating in this region have the capability of operating in the pA range. By operating entire systems in this operation region, huge power savings can be accomplished.

1.2 Signal Processing

1.2.1 Traditional Signal Processing

Traditional processing involves taking a continuous voltage, or current signal, from a sensor such as a microphone or a seismometer. From here, the signal will pass through an amplifier to reduce or increase the amplitude of the signal. Next the signal passes through a filter to cut-off some frequency content or reduce the level of noise in the signal. After the signal is “conditioned”, an analog-to-digital converter

Figure 1.1: Traditional interface between sensor and mote involves converting the sensor data into the digital domain prior to processing by the microprocessor. In the new proposed system, analog pre-processing is done using an ASP. Here information is determined to be relevant or irrelevant. If the information is determined to be important, the information is converted to digital and then additional processing is done by the microprocessor. This will in turn save energy since the microprocessor does not process all events.

is used to create a stream of bits for a microprocessor or Field-programmable Gate Array (FPGA) to process the information.

Using Digital Signal Processing (DSP) allows for a shorter development time than developing an application specific ASP system, and changes can be made much more easily. Unfortunately, DSP also puts all of the processing on the microprocessor, FPGA, or DSP chip, which consumes much more power than sub-threshold analog systems. Proposed here is an alternative solution to typical signal processing. Figure 1.1 shows a block diagram of a typical interface between sensor and mote, as well as the new proposed interface between an analog system and mote.

1.2.2 Analog and Digital Together

Since sensors data is an analog signal, analog pre-processing could be used to lighten up the processing done by the DSP. Doing so would save on energy costs due to the low operation points of analog circuits while maintaining the ability to do high level processing on the digital end by using the mote.

In this work, two analog event detector/classification systems have been created for use in wireless sensor networks. These networks require high energy efficiency due to their constrained power supplies. The first system contains a programmable analog filter bank and magnitude detector developed by Brandon Rumberg in [13], for use as a frequency content detection system. The second is a biologically based analog vision system with an adaptive photo-element for use in several different lighting conditions. A velocity detection system is also discussed for use in correlation with the vision system to detect object speed and direction.

1.3 Overview of this Work

Detailed in this work are several systems used for event detection and classification. The spectral analysis system discussed is used for use as a smart wake-up system for wireless sensor networks. The system contains analog filter banks and magnitude detectors created by Brandon David Rumberg in 2009 [13]. Mr. Rumberg's research work has been modified to create a frequency detection wake-up system for a wireless sensor network. I have included detailed information regarding my work on an analog vision system for use as a sensor in a wireless sensor network. This system is composed of a highpass filter, lowpass filter, Gilbert multiplier, and an adaptive photoreceptor cell. In addition, a new velocity detection system that can be used with the vision system is discussed. All of these systems are designed to work in low-power conditions.

1.3.1 Analog Spectral Analysis System

The spectral analysis system created by Mr. Rumberg contains several bandpass filters that have programmable center frequencies and quality factors. The bandpass filter bank circuit uses less than a μW at speech frequencies and also consumes less than a μW of power [13]. Adding a Complex Logic Device-based (CPLD) classifier enabled the circuit to become a programmable intelligent wake-up system for a WSN.

1.3.2 Analog Vision System

The biologically inspired vision system was created based upon the adaptive photoreceptor circuit developed by Mr. Delbrück [14], which allows the circuit to be used in a variety of lighting conditions, which enables the system to adapt to its new lighting environment. The vision system has a programmable velocity detection, so only objects moving within a certain range of speeds will be detected. This system was first developed in [15], and was constructed in order to study the vision system of a common house fly.

1.3.3 Velocity and Direction Detection

The velocity and direction detection sub-system is used in conjunction with the analog vision system. This sub-system contains mostly digital logic with some sub-threshold analog circuitry to create a well developed hybrid system. With this sub-system added to the already low-power vision system, direction can be obtained by observing a single bit output, while speed is achieved by observing an analog voltage.

1.3.4 Analog Intelligent Wake-Up

Typically, WSN use timers to keep a system low-powered, while sampling data from its sensors. Mote's typically remain in a sleep state, and awaken at a desired frequency to read data from its sensors prior to returning back to its low-powered

sleep state. There are two disadvantages of utilizing this wake-up and detect system. The first disadvantage is that sampling only at a desired frequency will lead to several missed events during the time when the mote is not polling its sensors. This can be solved by constantly keeping the analog sensors on. The second disadvantage is that on each sensor poll cycle, the mote is taken from its low-power sleep state to process all of the sensor data. This causes unnecessary power to be consumed by the mote's microprocessor and ADC. With the systems proposed here, motes remain in their low power sleep state until an event of interest is detected by the ASP. This saves power and uses the ADC to only interpret data of interest.

1.4 Related Work

The spectral analysis system was first conceived by Brandon Rumberg for his master's thesis in electrical engineering while attending West Virginia University. His research included work on creating a low-power front end for an auditory system. Currently in the lab at West Virginia University, a journal paper , [16], has recently been approved for publication on the works of a detect and wake-up system for vehicles as explained later in this paper in detail. The contribution being made is understanding how to use the system created by Mr. Rumberg, for implementing frequency detection wake-up for wireless sensor networks. Based upon the principles explored here, a similar technique is used for designing and testing this vehicle detection system.

The concept of motion detection was first researched by Reid R. Harrison and Christof Koch in [15]. Their work was conducted for research and study of the vision system of insects, in particular the common house fly. Their idea, concept, and circuit was taken from its current form and changed slightly for use as a motion detection system in a Wireless Sensor Network. For instance several new options were explored for the creation of a photo-diode which would work best for the type of application.

Also, the output of the circuit's final stage needed to be modified such to cause a single interrupt, instead of having two outputs per every single pixel.

The velocity and direction detection circuit was an original concept explored due to inadequate information from the original design by Reid R. Harrison and Christof Koch. Their implementation depended upon an object moving at a predetermined speed. If the object is not moving in the desired velocity range, the object will pass without notice. Also, although their design was capable of determining object speed, this could not be done unless all pixel outputs are observed independently. Therefore, the new system was created to cause a wake-up no matter how slow or fast an object's velocity was, and would be capable of determining the speed of the object. Also made capable in the new design was a way of determining the object's direction, which gives way to a more complex wake-up and detect system for wireless sensor networks.

1.5 Outline

In the next chapter, a brief description of the analog spectral analysis system designed by Mr. Rumberg is provided. An explanation of how the system is used to create an intelligent frequency detection system is also discussed. Chapter 3 presents the analog vision system and its components, along with how it is used for event detection, mote interfacing, and power consumption. The speed detection system and a description of how this circuit interfaces with a TelosB mote is described in Chapter 4. Chapter 5 discusses improvements made upon the first version of the vision system as well as future work possibilities. Chapter 6 concludes the document.

Chapter 2

Analog Spectral Analysis System

Microphones and seismometers are often used in systems to detect some type of signal or pattern. Systems such as these need to be left in a high power consuming state in order to detect all events, regardless of interest. These systems consume large quantities of power as time progresses. WSN motes using a battery as a power supply will not last long under these power strenuous conditions. Presented in this chapter is a low-power analog based spectral analysis system capable of pre-processing signals given by sensors such as a microphone or seismometer. By allowing ASP to take place prior to DSP, the mote can remain in its low-power sleep state with its ADC off, thereby consuming much less power resulting in a longer battery life.

2.1 System Background

The system discussed here uses a spectral analysis system composed of bandpass filters and a magnitude detector [13, 16]. The system developed in [13] was adapted to create a system in which only frequencies containing certain spectral properties would cause a mote wake-up and data transmit to a base station. The bandpass filters developed by [13] have programmable gains, center frequencies, and quality factors. After the signal is filtered by the array of bandpass filters, the signal travels

Figure 2.1: Block diagram of the entire system.

through an RMS (Root Mean Square) detection circuit. The overall goal is to create a detection system to identify when a signal matches a binary spectral template(s), which can be done using a bandpass filter array, magnitude circuit, and a CPLD as described in 2.1.

2.1.1 Bandpass Filter Bank

The bandpass filter bank is composed of eight total bandpass filters. The filters have been designed to obtain an input linear range of 200mV and for low-power, low frequency applications [13]. The bandpass corner frequencies are tunable through changing gains g_{m1} and g_{m2} , which are tunable by changing voltages V_{τ_l} and V_{τ_h} in 2.1. The transfer function of these filters is given by

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} \frac{s\tau_l (1 - s\tau_f)}{1 + s \left(\tau_l + \tau_f \left(\frac{C_0}{C_2} - 1 \right) \right) + s^2 \tau_h \tau_l} \quad (2.1)$$

where the time constants are described by

Figure 2.2: Schematic of the bandpass filter. The corner frequencies are electronically tunable and are independent of each other. They are established by biasing V_{tl} and V_{th} respectively.

$$\tau_l = \frac{C_2}{g_{m2}} \quad \tau_h = \frac{C_T C_0 - C_2^2}{C_2 g_{m3}} \quad \tau_f = \frac{C_2}{g_{m3}} \quad (2.2)$$

and $C_T = C_1 + C_2 + C_W$ and $C_O = C_2 + C_L$.

2.1.2 Resistive Divider

Several researchers have looked toward biology for inspiration in sensory systems. The cochlea is the front-end of the biological auditory system. A resistive divider network has been configured to implement a cochlea here in order to achieve desired spacing between the filters. Several systems have already been created using this same design technique as shown in [17, 18, 19, 20, 21]. The spacing between each filter bank is based on a log scale and can be achieved through a resistive divider network, shown in Fig. 2.3. This can be done since the circuits are biased in weak-inversion region there transconductance values vary exponentially according to there bias voltages.

Figure 2.3: Schematic of the filter array and biasing structure. Each of the eight filters receive the input signal in parallel. Two resistive lines are used to bias the corner frequencies of all of the filters. Since the filters are operated in the sub-threshold regime, linear spacing of the bias voltages translates into exponentially spaced center frequencies.

Therefore, two large resistive lines are used to generate the linearly spaced voltages for all V_{t_l} and V_{t_h} voltages. This can be tuned for the desired frequency ranges and spacing. Used for this particular application, $1/N$ octave spacing is used which is most commonly used for vibration and acoustical analysis. Figure 2.4 shows the ability to set the filter bank for one, two, or three filters per octave [22].

Since the resistive divider network is being used in coordination with a digital mote, programming the filter banks by using the mote becomes a very easy task by simply sending the new voltage values desired to the mote.

Although using a resistive divider makes it very easy to program the filter bank, there are some drawbacks. The accuracy of these filters depends on resistors being perfectly matched during the MOSIS fabrication, which in terms of matching is generally poor. Even though having the ability to program the divider network makes for easy filter bank updating, it also requires the mote DAC to remain on, causing a greater power draw. There is a solution to both of these issues involving the use of floating gate transistors and is discussed in [23].

Figure 2.4: AC response of the filter bank for: (1) octave spacing, (2) 1/2 octave spacing, and (3) 1/3 octave spacing.

2.1.3 RMS Detection

The output of the bandpass filter bank is passed through a peak detector and a lowpass filter in order to obtain the signal power in each of the eight bandpass filters. The peak detector of [24] was modified by Rumberg in [13] so that the output is slowly discharged via a constant drain through a transistor. This detector circuit performs the operation of rectification and is followed by the second stage, a G_m -C lowpass filter.

The lowpass filtering time constant can be adjusted to obtain the best possible compromise between accuracy and responsiveness as explained in [16].

2.1.4 CPLD

The output of all eight of these sub-bands are passed into a CPLD (Complex Digital Logic Device) where each sub-band is compared to a programmable threshold value. Each sub-band is then compared to a programmable threshold. If the magnitude of this sub-band exceeds the threshold, its bit is changed to a '1'. This in turn will create a single byte of data containing one bit from each of the eight sub-bands. This byte of data is then compared to a pre-programmed template, i.e. codeword(s), and if one of these codewords matches the current CPLD byte output, an interrupt is raised by the CPLD to the mote. Upon wake-up, the mote will use its ADC and a multiplexer to read the output of all eight sub-bands for a finite amount of time. This information is then transmitted to the nearest base station where further processing can be done.

2.2 Basic Frequency Detection System

In order to better comprehend how each of the sub-systems behave, we created a MATLAB program to simulate the response of each of these subsystems as shown in 2.5. With the aid of the MATLAB spectrogram plots, data could be visualized and became more easily interpreted.

By using the MATLAB program, bandpass parameters can be adjusted with ease and magnitude outputs could be compared similarly as if it were running on the actual spectral system. By using observation and iteration of the same set of signals, a frequency detector could be trained by using MATLAB.

2.2.1 Training a Detector

In order to create an actual event detector, signals were repeatedly run through the MATLAB program for different parameters of the bandpass filter and threshold

(i)

(ii)

(iii)

Figure 2.5: With the aid of MATLAB simulations, observing the response of the sub-systems became easier. (i) shows a spectrogram output, given a step response. (ii) shows the output produced by the array of bandpass filters, while (iii) shows the magnitude output of all eight sub-bands.

values of the comparator. Once a combination of parameters were found that would create an interrupt for only a desired frequency, the parameters were programmed to the actual system. Testing and minor adjustments could now be done in order to achieve the proper response of the system.

2.2.2 Basic Frequency Detection Results

Using the MATLAB iterative approach was determined to be the best way of finding exact parameter values. This proved to be much quicker than using the mote to control the parameter biases and then run tests due to the motes ability to only record one channel at a time, because of the multiplexers need to traverse all sub-band outputs. Figure 2.6 shows an example of a basic frequency detection system with a mote interrupt. These data, and all subsequent data (unless otherwise specified) were obtained from a $0.5\mu\text{m}$ CMOS integrated circuit.

Since the system has a possibility of being programmed for a total of 256 different frequency combinations, more than one single frequency can be detected and is shown in Fig.2.7. Even though this example shows instances of when only one sub-band has exceeded the threshold, it is possible to trigger an interrupt when more than one sub-band has exceeded the threshold at a given time. Such instances would require two bits being in their logic high state as opposed to one bit as shown in Fig.2.7.

The timing diagram shown in Fig. 2.8 shows in detail how the system behaves once an event of interest is detected. Take note that there is some lag time between when the event occurs and when the interrupt is triggered for the mote to come to a higher powered state. This behavior is caused by the RMS circuit and we explain it in detail in [16].

(i)

(ii)

(iii)

Figure 2.6: In (i), a 60Hz input signal added with random noise is passed into the system using a DAQ. (ii) shows the response of the bandpass filter array along with the interrupt passed to the mote, while (iii) shows the output of the eight magnitude responses as well as the interrupt output. The codeword used to program the comparator is set to '01000000', corresponding to the one bandpass filter that has a magnitude high enough to trigger an interrupt.

(i)

(ii)

(iii)

Figure 2.7: In (i) a chirp input with added noise is given to the system using a DAQ. The system has been pre-programmed for three different codewords which can be seen in (ii) and (iii) as the three different instances of the interrupt voltage. (i) once again shows the response of the bandpass filter array, while (iii) shows the response of the magnitude circuit for each sub-band.

Figure 2.8: Actual timing diagram achieved for frequency detection system. Signals were passed to the ASP using a DAQ. Outputs from the ASP were read in through the DAQ. Notice the delay time between when the event occurs and when the interrupt is triggered for the mote to come to a higher powered state. This issue is caused by the RMS circuit.

2.3 Vehicle Detection Application

By using the same basic principles as described above, the modern vehicle detection system described in [16] was developed. Using an acoustic-sensor based vehicle classification scenario and data collected for use as described in [25] the detection system was trained. In [25], the vehicles are assumed to appear in isolation and not in correlation with other vehicles at the same instant. The system was created to classify vehicles into two separate categories, car or truck, and would ignore frequencies detected but not of importance.

2.3.1 System Data and Training

Two vehicles were used in this system. They consisted of a mid-sized car (Honda Accord LX) and a pickup truck (Chevrolet C4500 4x4). Each vehicle was driven at speeds varying between 10 mph and 30 mph. The sound of each vehicle was recorded using a USB Studio Condenser Microphone sampled at 4kHz as described in [25]. In addition to the sound clips of the vehicles, ambient sound was collected without any vehicles present.

The training of the system began by separating the data into two separate classes, one for training and one for testing use. All data was normalized as explained in [16]. Regions of the data where the vehicle is actually present were manually identified.

The filter bank of the analog circuit was chosen for half-octave spacing from 100Hz to 1131Hz based on short-time FFT spectra of data, which was computed using Matlab Simulation Software. Analysis was then performed by streaming all of the training samples through the ASP using a DAC and then recording the RMS output of each band of the filter bank. From here, observations were made to determine which code word would trigger an interrupt using the 8-bit combination as explained earlier in this chapter.

Once all of the data was analyzed, training the detector (finding the code words for each class and appropriate threshold value) is done using an iterative approach as we explain in [16] and previously in this chapter. Once these assignments are made, the system is configured by programming the code words into the CPLD and transmitting the threshold value to the mote. The CPLD is programmed such that the interrupt pin goes high upon receiving a codeword associated with a car or truck and the classification pin goes high for each truck encountered.

In order to compensate for false decisions created by the ASP due to instantaneous signal-to-noise ratios, the mote is used to generate the final classification (i.e car or truck) output, based on outputs from the ASP over a finite amount of time. After

Figure 2.9: Stages of vehicle detection system. The truck is closest to the sensor between 4-6 seconds, shown in (ii). The spectral output of the input is shown in (iii). Shown in (iv) is the 8-bit output of the comparators followed by the CPLD interrupts and CPLD classification in (v). The power consumed by the entire system is shown in (vi).

the mote receives an interrupt, it waits for the interrupt pin and the GPIO pin to remain low for 100ms to verify that the vehicle is outside of the detection range. The mote will then give the final decision based upon the most frequent codeword from the ASP over the duration of the interrupt.

2.3.2 Results and Digital Comparison

Each test was conducted by streaming the samples through a 16-bit DAC and into the ASP at a sampling frequency of 4kHz. Figure 2.9(i) shows the input to the system (a ten second sample of a truck). The vehicle presence is shown in Fig. 2.9(ii) and the spectral analysis of the sample is shown in Fig. 2.9(iii). The output of the comparators, the codeword, is shown in Fig. 2.9(iv), followed by the output of the CPLD interrupt pin and CPLD classification pin in Fig. 2.9(v) and Fig. 2.9(vi). The last graph indicates the power consumed by the entire system as well as the power consumed during the motes transmit in Fig. 2.9(vii). The radio transmit consumes roughly 60mW of power while the actual CPLD consumes only 1.5mW. Table 2.1 shows an overview of all the tests conducted on this system. An overall accuracy of 90% was achieved with an average false positive every 50 seconds in the presence of amplified ambient win noise [16].

For comparison against an all digital system, a Mica2 mote with an attached seismic sensor stays on all the time in order to detect the arrivals of a vehicle as described in [26]. Upon detection, a Linux based Stargate platform is awakened and performs the spectral analysis necessary for vehicle classification. The mote uses 1.5mW of power and must remain on continuously in order to detect all interesting events and uses 60mW of power when transmitting. The Stargate, using a 4.2V battery, uses 420-470mA when processing for a duration of 8-10 seconds whenever a vehicle detection is made. In comparison the analog-digital system described uses 417 μ W of power when idle, and 1.5mW of power when an event is detected.

Table 2.1: Vehicle Classification Results

	Ground Truth		
	NULL (200 seconds)	Car (10 Samples)	Truck (10 Samples)
NULL		20%	0%
Car	2 false alarms	80%	0%
Truck	2 false alarms	0%	100%

Figure 2.10: The power consumed by the analog spectral-decomposition block depends primarily on the center frequency of the bandpass filter of the highest frequency sub-band. The x-axis shows the center frequency of the highest-frequency sub-band for an array that performs spectral analysis. Also included are power measurements from the digital mote including the minimum measured power consumption in sleep mode.

2.3.3 Power Consumption

The main power draw of this analog circuit comes from the bandpass filters, while some comes from the magnitude circuit. The power consumed by the bandpass filter is linearly proportional to the highest center frequency. Figure 2.10 shows this data for a filter tuned to 1 octave, along with the amount of power dissipated by a TelosB mote in its sleep state ($25.4 \mu\text{W}$), and the power consumed by a digital bandpass filter. As shown in the Fig.2.10, the power consumed by the analog spectral-decomposition block is set by the center frequency of the highest filter tap [16]. The total power of the entire system is described by

$$P_{tot} = \frac{P_{BPF,high} + P_{RMS,high}}{1 - 2^{-1/N}} \quad (2.3)$$

where N represents the number of filters per octave, $P_{BPF,high}$ and $P_{RMS,high}$ represent the power consumed by the BPF and RMS circuits in the highest-frequency sub-band. As shown, the entire analog block uses less power than a sleeping mote.

In conclusion, this system uses very little power in comparison to the all-digital system. This system has shown a great benefit for applications where vehicle detection happens at a very rare rate. This application is likely to be beneficial in more general classification scenarios with more than 2 class types as well.

Chapter 3

Analog Vision System

Camera networks used as security systems are typically on during certain intervals throughout a given period of time. Camera network systems used to provide surveillance, require large amounts of power to keep all the cameras in the network on for a given period of time. In addition to the considerable amount of power required to run this type of system, an extraordinary amount of storage space is necessary. The cameras used in these situations typically record data to some external data storage unit; with several cameras recording various angles. Presented in this chapter is the use of an analog biologically inspired vision system for waking up a higher power camera network. By using this low power analog-based vision system, cameras can remain in an off state until motion is detected at a programmable speed, resulting in saved storage space and energy. Cameras will remain powered off until motion is detected which requires less storage space to be used.

3.1 Circuit Realization

The vision system described here is based on the work conducted by Harrison and Koch in [15]. In [15], research was conducted in order to model and study the vision system of the common house fly. However, in this work it is used as a low-power

motion detector for intelligent wake-up in a wireless sensor network.

The analog vision system is driven by an array of photoreceptor cells, high and lowpass filters, and Gilbert multiplier circuits. Figure 3.1 shows a block diagram of a three-pixel array of photoreceptors. Each of the photoreceptors in the array is responsible for continuously monitoring light intensity. When an object passes through the field of view of one of these receptors, a large change in intensity occurs. A highpass filter is used to take the large change in intensities and create a “spike” in the signal. This spiked signal is then correlated with a delayed version of the spiked signal from an adjacent photoreceptor cell. This is done in hopes of “seeing” the object crossing the view of an adjacent cell at a later time. Correlation of these two signals is done by using a Gilbert multiplier. The output of the Gilbert cell is typically a current. While no motion is detected, this current is a continuous DC current. Once motion occurs, the current output of the cell decreases. This current is changed into a voltage by using a diode-connected MOSFET transistor. If this voltage exceeds a programmed threshold and interrupt is raised, the mote is awakened from its sleep state. The first step in being able to detect motion is to convert incident light into some kind of physical signal.

3.2 Diode Selection

Several different diodes and photo-transistors were created in a $0.5\mu\text{m}$ process in order to determine which was best suited for this type of application. Testing was conducted on each to find its respective responsiveness to changes in light. A flashlight was used as a constant light source to each of the diodes/BJT's while the current through each of the devices was read using a DAQ and MATLAB simulation software. This gave a baseline for each of the devices determining how much each could sink. Objects were then placed in front of the flashlight during testing for each of the devices. This testing determined the range of current values that were achieved

Figure 3.1: System Diagram. Each photoreceptor output is passed through a high-pass filter before being delayed by the lowpass filter. The lowpass filter output then becomes correlated with an adjacent pixels highpass filter output, by using a Gilbert multiplier circuit. The output of the multiplier is a current which is converted into a voltage by using a simple diode connected Field Effect Transistor (FET).

for each diode/BJT. The device showing the largest current fluctuations for the two light contrasts was chosen as the device to be used in this system. The device chosen was a $26\mu\text{m} \times 26\mu\text{m}$ p-n junction diode created in an n-well as shown in Fig. 3.2. Terminal V_{in} is to be reversed biased to terminal I_{out} . A larger sized P-type material is created in order to give a better area for photons to hit and create a larger amount of electron-hole pairs.

3.3 Photoreceptor Cells

The photoreceptor used here is a $26\mu\text{m}$ by $26\mu\text{m}$ n-well photodiode. This photoreceptor circuit uses a four transistor scheme with a feedback system which amplifies the signal by a factor of 18 [15], and is shown in Fig. 3.3. The photo-diode is reverse-bias connected to the source of a nFET which converts the incident light into a logarithmically encoded voltage. Transistors M_2 and M_3 along with C_1 and C_2 form a high gain

Figure 3.2: Photo-Diode layout photograph. The size of the diode is $26\mu\text{m} \times 26\mu\text{m}$ and contains a large P-type material in comparison with the N-type material.

common source amplifier, where the ratio of these two capacitors helps determine the gain of the circuit. The input voltage to the circuit, V_{pr} determines the current which is sourced by transistor M_3 . This voltage also determines the cut-off frequency of the photodiode by setting the bias current in the inverting amplifier, which can be used to eliminate the flicker in artificial lighting elements [15]. The DC level of the output can also be adjusted to a desirable level by shifting V_{pr} up or down as shown in Fig 3.4.

As described in [15], the photoreceptor response can be modeled as

$$H(\omega_t) = \frac{K j \omega_t \tau_{HPF}}{(j \omega_t \tau_{HPF} + 1)(j \omega_t \tau_{photo} + 1)} \quad (3.1)$$

where τ_{HPF} is the time constant of the associated highpass filter, τ_{photo} is the time

Figure 3.3: Adaptive photoreceptor circuit.

constant describing the photoreceptor bandwidth, K is a constant of proportionality, and

$$\omega_t = 2\pi v f_s \quad (3.2)$$

where f_s is the spatial frequency, and v is the velocity at which the object is moving.

3.3.1 Adaptive Element

Transistor M_4 is used as an adaptive element and only conducts appreciable current when the voltage across it exceeds several hundred millivolts. This allows for use in a wide variety of lighting conditions, while still maintaining a large operating range.

Adaptation occurs when charge is taken off or placed on capacitor $C1$. The adaptive element acts like a pair of diodes having opposite polarities and the current has

Figure 3.4: The system was simulated using Cadence spectre simulation software. A step input current in place of the photoreceptor as shown in (a). The output voltage relative to the bias voltage V_{pr} is shown in (b).

an exponential relationship to an increase in voltage at either end. This I-V relationship indicates that for a small signal input, this element acts as a large resistance and for a large signal input, the element acts as a small resistance. This characteristic works extremely well for this application because it will adapt very quickly for large changes in light and will still have high sensitivity to small changes in light. This I-V relationship is shown below in Fig. 3.5. A more in depth look at the adaptive element can be found in [14].

Figure 3.5: I-V characteristic curve for photo-adaptive element.

3.4 Highpass Filter

The highpass filter circuit serves several functions, but most importantly is used to create a “spike” in the analog signal when a difference in light intensity has been detected. The highpass filter circuit is shown in Fig. 3.6. Initially the signal is sent to a source follower for use as a low-impedance driver. The bias voltage V_{SF} sets the

Figure 3.6: Highpass filter circuit schematic.

DC output level of the source follower as shown in Fig. 3.7.

First, the AC coupling after the source follower will eliminate offsets due to device mismatch in the previous photoreceptor cell. Second, by setting a DC level to voltage V_a , any common-mode effects later on in the circuit are eliminated. The most important function of the highpass filter is to serve as a differentiator for incoming signals. The highpass filter will create an upward or downward going “spike” in the output signal. This “spike” represents a change in the light intensity by the photoreceptor, and is shown in Fig. 3.8.

By changing the bias voltage V_{lpf} , the corner frequency of the filter can be shifted

Figure 3.7: Simulated source follower characterization curve. Note, as V_{SF} increases, V_{out} decreases.

to a desired value as show in Fig. 3.8. This will determine the time required by the highpass filter to return to its steady state output. Typically, this value is set to have the fastest response possible in order to detect the next change in light intensity.

After the signal traverses through the highpass filter, it becomes the input to a lowpass $G_m - C$ filter. Later on, this same highpass filter output will be multiplied by an adjacent photoreceptors lowpass filter output in a Gilbert multiplier circuit, discussed later on.

3.5 Lowpass Filter

The lowpass filter is used to accomplish a time delay. The lowpass filter used here is a standard $G_m - C$ filter and is shown in Fig. 3.9. By changing the voltage v_t the corner frequency can be adjusted, as shown in Fig. 3.10. This value can be adjusted

Figure 3.8: Shown in (i) is the actual highpass filter frequency response for several V_{hpf} bias voltages. Bias voltages were changed using a DAQ while a DSA would find the frequency content needed to obtain the magnitude of the frequency response. In (ii), the step response of the HPF is shown. As the bias voltage increases, the downward slew rate of the filter is much faster as demonstrated in (ii). This gives the ability to create a desired response time. This will play an important role when used in coordination with a lowpass filter, which is discussed later.

Figure 3.9: Lowpass filter circuit schematic.

in order to accomplish the appropriate delay relative to a desired speed detection system.

Objects moving at a slower speed require a larger time constant (larger phase shift) in order to shift the response further along in time. Faster moving objects however, need a smaller time constant and a smaller bias voltage. Using this methodology, the system could be tuned to detect objects moving only at desired speeds, while ignoring objects at other speeds.

The source voltage, V_{tilt} , is set a few tens of millivolts below V_{dd} in order to lower the DC offset at the output of the lowpass filter by a value of $(V_{dd} - V_{tilt})\kappa$ where $\kappa \approx 0.7$. By doing so the time constant of the lowpass filter is increased but compensation can be made by raising I_τ . This offset between the voltages also has some effect on the positive and negative slew rates of the filter, however this does not have a significant effect on this circuit's application.

Figure 3.10: Shown in (i) are the actual LPF step responses. Note that as the value of V_t changes, the rise time increases. With this in mind, the system can be tuned to detect only a desired range of speeds by increasing the time constant for slower moving objects or decreasing the time constant for faster moving objects. A DAQ was used to output several bias voltages, for each a step was given to the lowpass filter, while the output was recorded using the DAQ. Shown in (ii) is the actual highpass filter frequency response for several V_t bias voltages. Bias voltages were changed using a DAQ while a DSA would find the frequency content needed to obtain the magnitude of the frequency response.

Figure 3.11: Gilbert multiplier schematic.

3.6 Gilbert Multiplier

The Gilbert cell is used to multiply two adjacent pixel output voltages, in which one voltage is time delayed. The Gilbert multiplier consists of two sets of differential amplifiers followed by a third, as shown in Fig. 3.11. Voltage V_2 comes from the output of the lowpass filter and V_1 is the output of an adjacent pixels highpass filter output. The bias voltage V_a is the same bias used to set the DC level of the highpass filter and V_b is set a few millivolts below this value. The reason for V_b being set below V_a is because in order for the multiplier to work properly, the common mode voltage of the lower inputs (V_2 and V_b) must be lower than the common mode voltage of the upper inputs (V_1 and V_a). This is another reason for lowering the supply voltage, V_{tilt} , of the lowpass filter.

The circuit works as a big differential amplifier. Voltage V_1 and V_a are assumed

Figure 3.12: Multiplier common mode input voltage sweeps. Note that an upper common mode voltage greater than $\approx 50\text{mV}$ above the bottom input common mode voltages causes the multiplier to saturate. However, within this 50mV range the multiplier has a linear response. Output voltages were sent through the ASP using the DAQ, and the resulting output voltage was read using the DAQ.

to be at the same potential during its steady state, because the output of the HPF is set to V_a . When motion is detected, voltage V_1 will increase and cause more current to flow through transistors M_4 and M_7 . At the same time, if the circuit is tuned correctly, the lowpass filter output voltage V_2 will also increase causing more current to flow through transistor M_2 . This is described by

$$I_{out} = \frac{I_b}{2} + \frac{I_b}{2} \tanh \frac{\kappa(V_1 - V_a)}{2U_t} \tanh \frac{\kappa(V_2 - V_b)}{2U_t} \quad (3.3)$$

where U_t is the thermal voltage. From here, one can see that the circuit output saturates at $4U_t \approx 100mV$ and is shown in Fig. 3.12, and rather than limit the output, this nonlinearity is used as an advantage, as explained in [15].

The current output of the Gilbert multiplier is converted to a voltage and this is used for mote wake-up. The number of these output voltage will vary pending the number of pixels to be used in the system. For an array of ten photoreceptors there will be a total of 18 output voltages from several different multiplier circuits.

3.7 Motion Detection

As described in the above sections, motion is detected when the correlated outputs of highpass and lowpass filters are large enough to notice a change in current through the Gilbert multiplier. This is accomplished by first changing incident light into a logarithmically encoded voltage by use of Tobi Delbrück's adaptive photo-circuit [14]. This voltage signal is passed to a highpass filter, which creates a "spike" in the signal where the motion has occurred. A delay in the signal is then accomplished by using a lowpass filter. The delayed signal is then correlated with an adjacent pixels highpass filter output. Correlation is accomplished by using the Gilbert multiplier, and if a large enough change in the output current is observed, an interrupt is raised. Several output steps of the system are shown in Fig. 3.13, which shows the results of actual outputs of the systems components while motion is detected. For this experiment,

Figure 3.13: System output for basic motion detection system. A flashlight was used in order to obtain better visual results for the output of the photoreceptors. A hand was moved into and out of the range of the photoreceptors totaling four times, triggering four different interrupts to the mote. Outputs of the HPF, LPF, Photoreceptor cell, and as the motes interrupt pin were read using a DAQ.

a flashlight was used in order to give a large change in light intensity, while a hand was crossed between the flashlight and the photoreceptor cells. Figure 3.13 (i) shows the output of the photoreceptor circuit. Shown in Fig. 3.13 (ii) is the output of both the lowpass filter and adjacent highpass filter. The two outputs almost overlap one another due to the lowpass filter being a time-delayed version of the highpass filter output. Fig. 3.13 (iii) shows the interrupt pin of the system. Take note that the pin remains at a logic high state until the highpass filter and lowpass filter signals decrease.

3.8 System Interfacing

This system was used to wake-up a small-sized camera network using a Beagle Board. The Beagle Board is a low-cost, single board, fan-less computer produced by Texas Instruments. A single SD/MMC card is used to contain the operating system as well as any memory storage needed in coordination with the Beagle Board. The device also contains several GPIO pins used for interfacing with external circuitry. One of these GPIO pins was used in order to monitor the output of the vision system. A program was created in order to continuously poll the interrupt pin of the vision system. Once the Beagle Board notices a change in the status of the GPIO pin it turns on a small USB powered camera. The camera then captures images at 12 fps and stores each of these on the SD/MMC card. This operation continues to occur until the polling pin receives another interrupt from the vision system. On the second interrupt received by the Beagle Board, the camera is shut down and recording is ceased.

3.9 Power Consumption

A 1x10 array of these vision pixels was simulated using Cadence Design Studio. It was determined that power draw for the entire system was dominated by the constant current flowing through each of the photoreceptors as well as the constant current flowing through the Gilbert multiplier. Table 3.1 shows the results of the simulation in detail. The array uses only $11.72\mu\text{W}$ when motion is not being detected, and even less during an event. This is because the current through a photoreceptor is less when a dark object is over it. With this in mind, the system would become very useful and ideal when motion is anticipated to be detected frequently, due to its minimal power consumption. Even when the system is not detecting motion, it still uses much less power than a mote in its sleep state. When being compared to a PIR (Passive

Circuit	Motion Detected	No Motion Detected
LPF	2.9471 ρ W	3.6313 nW
HPF	1.8309 nW	0.937 nW
Photo-Cells	4.3834 μ W	5.4787 μ W
Multiplier	6.1898 μ W	6.2383 μ W
TOTAL	10.578 μ W	11.722 μ W

Table 3.1: Power Consumption Overview. Each circuit is broken up into how much power it consumes when no object is present and when an object has been detected.

Infrared sensor) sensor as used in home security systems, the system presented here uses much less current. A single PIR sensor uses around 50μ A of static current, which is much more than the static current used by the entire vision array system presented here. A system containing a Logitech QuickCam S5500 is said to consume 0.6W of power due to the camera only [27]. When being compared to this single USB powered camera this system uses much less power during its sleep state, then a single USB powered camera.

Chapter 4

Velocity and Direction Detection

The vision system discussed in Chapter 3 was a very low-power way to detect one-dimensional motion and can only be tuned to detect objects moving at certain velocities. However, specific object velocity as well as object direction would be extremely useful for higher programmability in low-power wake-up systems. Recall the example discussed in Chapter 1 with the surveillance system. By only using the vision system described in Chapter 3, motion within a tuned velocity range, regardless of direction, will cause a camera network wake-up. However, what if the object moving is in a direction that is away from the surveyed area? What if the type of motion detected is not of interest, or the system needs to detect all motion and not just certain velocities? With only the vision system running the wake-up, the camera network will awaken as long as the object is moving within the tuned velocity range. However, with the velocity detection system developed here, specific velocities as well as direction, can now be a part of constituting a wake-up.

4.1 Velocity and Direction Detection

The velocity and direction detection system is composed of a mixture of analog and digital circuitry. The main goal is to achieve some type of analog output voltage

which can be used to determine object speed, and direction. The system is composed of a nine transistor OTA (Operational Transconductance Amplifier), a highpass filter, two basic flip flops, a pulse generator, and several basic logic gates as shown in Fig. 4.1. The same photoreceptor circuit discussed in Chapter 3, is also used here to detect differences in light intensity. However, this output voltage will now be inverted using a nine transistor OTA with a bias voltage set around the steady state output of the photoreceptor. The OTA is used in order to detect changes in light intensity and flip the signal from downward slope to an upward slope. The signal passes to a highpass filter where again a “spike” is created in the signal. This spike is then used to drive digital logic circuits to a high input state. This highpass filter output, along with an adjacent highpass filter output, become the inputs to an OR gate. This OR gate is used to take the two input signals and make them a single output. This output is then used to drive the clock of a J-K flip-flop. The output of this flip-flop will remain low until the first pulse from the OR gate is seen. On the first pulse, the output state changes to high and a separate circuit will begin to linearly discharge a capacitor. Once the second pulse comes the flip-flop will return to its low output steady state. The voltage on the discharging capacitor can then be used to determine the speed of the object. An asynchronous reset pulse can then be used to reset the capacitor value back to its original state to prepare for the next motion detected.

A direction bit is either set or reset by using the information obtained at the output of the highpass filters. By using a combination of inverters and AND gates, the photoreceptor which has seen motion first can be determined. Knowing this information, a separate J-K flip flop is either set or reset depending on the output of this logic circuit.

A separate time-out circuit is used to prevent the system from remaining in a capacitor discharge state. The time-out circuit consists of a monostable pulse generator, an inverter, and an AND gate. On the first rising clock edge to the J-K flip flop, the pulse generate is taken to a high output state. The length of this state is

Figure 4.1: Block diagram of the speed detection circuit. The two comparators are used to detect when motion has occurred. The highpass filters serve as derivative circuits to produce an impulse response. The OR gate, which connected the two highpass filters, is used to drive the clock input of the J-K Flip Flop. The flip flop will enter an active high output state when the first pulse comes, and will return to its low state after the second pulse. During the active high time a capacitor is discharged from V_{dd} .

programmable by changing the bias voltage on a pFET transistor. Once the pulse generator returns to its low output state, it checks to see if the output of the flip flop is still in a high output state. If these two conditions are simultaneously met, the flip flop is given a forced pulse to its clock in order to return it to its low output state.

A detailed description of each of these circuit elements as well as how they each play the role of velocity and direction detection is provided.

Figure 4.2: Schematic of nine transistor OTA.

4.2 Operational Transconductance Amplifier

The nine transistor OTA is used as a comparator circuit as shown in Fig. 4.2. The non-inverting terminal of the amplifier is biased at the same potential as the DC output voltage of the photoreceptor circuit shown in Fig. 3.3. This steady state DC offset will need to be configured and biased, based upon the lighting conditions of the environment that the system is currently placed in. The inverting terminal of the transistor is connected to the output of the photoreceptor circuit. The reason the input to the inverting terminal is connected to the output of the photoreceptor circuit is because the voltage change when motion occurs is lower than its steady state voltage, shown in Fig. 3.4. This type of OTA configuration will invert the output of the photoreceptor, which is needed for the highpass filter input.

V_{Dis} mV	Discharge Rate $\frac{mV}{mS}$
500	116.43
483	86.94
467	63.99
450	46.2
433	33.15
417	23.34
400	16.23
383	11.32

Table 4.1: Several bias voltages for V_{Dis} and the resulting discharge rate found by using Cadence spectre simulation software.

4.3 Highpass Filters

The HPF is needed only for the purpose of finding the derivative of the input, which will create an impulse at the output of the filter. This will occur when the photoreceptor circuit's output voltage causes a state change in the output of the OTA. The DC output level of the HPF is biased to be as close to ground as possible, $\approx 200mV$, while still maintaining proper functionality. The DC level is biased such that its steady state output will be interpreted as logic '0' for the digital logic that follows. The HPF is also biased to have the quickest time constant possible while maintaining the output peak above $1.65V$ for logic high interpretation. This is done in order for the logic circuits to detect two rising edge logic pulses. If the HPF is not biased properly, pulses could be misinterpreted as one longer sized pulse, rather than two separate pulses. The fastest response of the HPF, achieved in simulation, enabled two separate pulses to come as close as $100\mu S$ of each other while still being considered two separate pulses. The output of the HPF drives the output of a basic OR logic gate.

4.4 Digital Circuitry

Two adjacent photoreceptor HPF outputs become the logical inputs for an OR gate. The logic gate is used to combine two separate analog signals into one digital signal. Since the purpose of the HPF's is to create a "spike" in the signal, this "spike" must raise high enough to be considered a logic '1'. On the first "spike" input to the OR gate, the output goes high, which drives the clock of a J-K flip flop and sets the output of the flip flop to logic '1'. This output is used to control a capacitor discharge circuit, which is discussed later. On the second "spike" created by the HPF, the J-K flip flop returns to its steady state of logic low. A safety time-out circuit is created in order to cover certain probable states which can accrue over time. This circuit, discussed in a later section, is used to also control the output status of the flip flop. It is used to bring it to its steady state of logic low after a programmable amount of time after the first "spike" occurs.

4.4.1 Capacitor Discharge Circuit

The output of the J-K flip flop is used to control transistor M_1 and M_4 of Fig. 4.3. When the J-K flip flop is in its set state, logic 'high' output, transistor M_1 is off and M_4 is on thus discharging capacitor C_{Speed} through transistors M_3 and M_4 in Fig. 4.3. The discharge rate of the capacitor is controlled by transistor M_3 and is summarized in Table 4.1. The capacitor continues to discharge until one of two things occur. Either the flip flop is returned to its normal reset, logic 'low' output, by the second pulse from the OR gate, or the output of the flip flop is forced to its low state by a timeout circuit, which is described below. Once the flip flop returns to its logic low state, the analog voltage on the capacitor remains at its current value until a pulse is received on transistor M_2 . This pulse input is needed to ensure that enough time has passed for the mote to use its ADC to read the capacitors voltage, before being reset to V_{dd} .

Figure 4.3: Schematic of capacitor discharge circuit. M_1 and M_4 are inputs from the J-K flip flop. The bias to transistor M_3 controls the discharge rate of the capacitor. Transistor M_2 needs a positively edged pulse to reset the capacitor value to V_{dd} .

Figure 4.4: Circuit schematic for pulse generator time-out circuit.

4.4.2 Circuit Time-Out

The time-out used here serves to bring the system back to its steady state response so event speeds are not missed. Several scenarios exist for when the time-out would be needed, including single pixel motion detection and slow moving objects. The time-out circuit is a digital monostable multivibrator circuit. It is made by creating two NOR gates back to back, as shown in Fig. 4.4. The trigger input is taken as the output of the J-K flip flop. The pulse generator works initially having NOR gate N1 have an active high output, therefore capacitor C_{Pulse} has the same charge on both of its plates. NOR gate N2 at this point acts as an inverter and its output is a logic '0'. When the trigger input to N1 becomes positive, it produces a logic '0' output and thereby discharges the capacitor to ground. N2 now has a logic '0' input and has a logic '1' output, and will remain this way until capacitor C_{Pulse} is charged back up through transistor M_1 . The gate voltage on M_1 controls how quickly this charge up will occur, and therefore, the output pulse width can be controlled via this bias voltage therefore, different time-out periods are achieved.

The output of the pulse generator is inverted and becomes the input to an AND gate along with the output of the J-K flip flop. Therefore, if the pulse expires and the output of the flip flop still remains in a logic '1' output, a forced pulse is given to the J-K flip flop by the output of the AND gate.

The time-out circuit is used in order to cover several scenarios all of which are

likely to occur at some point during system operation. One such scenerio is having motion detected by one pixel however not the second. This case is likely if an object is to move into view of one pixel and then out of view, which is important for pixels on the edge of the array. In this case, motion is perceived by one pixel but never the second. Another instance in which this is useful is when an object is moving to slowly through the field of view. In this instance it is important to have a time-out to catch the speed of a possible faster moving object. Furthermore, if the light intensity changes at one pixel and not the other, such as lighting condition changes in the environment, this time-out will return the system to a stable state.

4.4.3 Direction Detection

The object's direction is determined with the use of another flip flop. The output of the flip flop, whether set or reset, depends on the object's direction. The direction bit is determined as soon as the initial pixel detects motion. The output of one highpass filter is ANDed with the inverted output of the other highpass filter output. By using this methodology, the output bit of the flip flop will either have a state of logic high representing one direction, or a logic zero, representing the opposite direction.

4.5 Mote Interfacing

Interfacing this system to a mote requires access to the mote's ADC pin, two general IO (Input/Output) pins, and an interrupt pin. The mote's ADC pin is used in order to accurately read the voltage of the capacitor. By using the peset capacitor voltage level, the object's overall velocity is directly correlated to its linear discharge. One of the general purpose IO pins from the mote will be used to reset the system's velocity capacitor C_{Speed} (Fig. 4.3) back to V_{dd} , while the second will be used as an input in order to observe the direction the object is currently moving. The mote's

interrupt pin should be connected to the output of the flip-flop used to discharge the capacitor, and should be set to interrupt on a falling edge input. This method is used to trigger the interrupt when the capacitor value is ready to be read using the ADC on the mote.

This system was built on a breadboard and was given inputs using a DAQ (Data Acquisition System). The DAQ was used to simulate changes in voltage levels seen by each HPF. The mote was setup to have a negative edge triggered interrupt and was connected to the main flip-flops output pin. With this setup, as soon as the capacitor finished its discharge, the mote would receive an interrupt. After receiving the interrupt the mote would sample its ADC pin, record the value, and send it to another mote running as a base station. The base station was connected to the USB port of a computer running Linux. Through serial communication, the value received by the base station mote would be displayed in hexadecimal on the terminal of the computer. Each hexadecimal increment represented $\approx 50\mu V$. During a single test a value of “0D D7” was the result which was read by the ADC and displayed on the terminal which translates to a value of $\approx 3.12V$. Now, knowing the capacitor has discharged by $\approx 0.18V$ and the distance between the two pixels, the velocity of the object can be determined.

4.6 System Performance

The velocity system is capable of detecting motion for three separate scenarios; motion moving from left to right, motion moving from right to left, and motion detected by one pixel however not an adjacent pixel. Figures 4.5, 4.6, and 4.7 show simulated results using cadence design software. Figure 4.5 shows an example of motion simulated from the left to right direction. In (i) of this figure shows the change in current from two adjacent photoreceptor cells, note that the DC current level shifts from a higher level to a lower level. This is because as objects pass over

each pixel, the current through these devices will decrease. Subfigure (ii) of Fig. 4.5 shows the output of both HPF's, note that the filters create a positive "spike" in the signal. Subfigure (iii) shows the capacitor charge of C_{Speed} in Fig. 4.3. Note that as soon as the first "spike" of subfigure (ii) reaches a high state, the capacitor begins to discharge until the second spike is detected. At $\approx 170\text{mS}$ a pulse is given on transistor M_2 in order to reset the voltage level of the capacitor back to V_{dd} . Figure 4.5 (iv) shows the directional bit output of the system. For this scenerio the bit is set, while in Fig. 4.6 the direction bit is reset. Lastly, Fig. 4.5 (v), shows the pulse width of the time-out circuit. For this scenerio it is not needed since motion is detected by two adjacent pixels, however in Fig. 4.7 it is required in order to place the output back to its steady logic zero state. Note also that in Fig. 4.7 (iii) the capacitor continues to discharge until the flip flop is returned to its steady state by the time-out pulse. Furthermore, in Fig. 4.5 (v) and Fig. 4.6 (v) the reset pulse remains at a logic zero, while in Fig. 4.7, the reset pulse reaches a logic '1' due to motion not detected by a second pixel.

4.7 Power Consumption

The average energy consumption of this circuit is dominated by the programmed pulse width. As the pulse width of the circuit increases the average energy consumption of the circuit increases. This is shown in Fig. 4.8. When using this system to detect slower moving objects, a larger time-out pulse width is required. However for a faster moving object, a shorter pulse width is required in order to be in its stable state for the next motion to be detected. In each case, even with the pulse programmed for its smallest period width, the velocity detection system still consumes less power than a mote in its sleep state at $\approx 3\mu\text{ J}$, shown in Fig. 4.8. The amount of current consumed by this system is less than the current used by a single PIR sensor and the Logitech QuickCam S5500 as discussed in Chapter 3.

Figure 4.5: Timing diagram for object moving from left to right, with a separation of 10mS . The system is given a current step input change to simulate a change in light intensity detected by the photoreceptors. Subfigure (ii) shows the response of the HPF circuit, while (iii) shows the output of the flip-flop. Note that the output of the flip-flop goes high on the first motion detected and goes back low for the second pulse. During this interval of time, the capacitor is discharging, shown in subfigure (iii). The output of the direction bit is shown in (iv). Here, a logic '1' represents motion from right to left. The pulse generator used for the system time-out is shown in (v) along with the reset bit. The reset bit is never high because the second pulse comes while the pulse generated is still in a high logic state.

Figure 4.6: Timing diagram for object moving from right to left, with a separation of $10mS$. Each subfigure shown here is identical to those shown in 4.5, with the exception of (iv) which shows the direction bit now flipped to a logic low. This indicates that motion has occurred in the opposite direction, right to left.

Figure 4.7: Simulated timing diagram for motion detected by one pixel, but not an adjacent pixel. In (i), only one of the inputs go low. Simulated motion is detected by one pixel, but not the adjacent pixel. As such (ii), only shows that one HPF responds to the change in light intensity. Subfigure(iii) shows that the capacitor will continue to discharge until the system time out responds. (iv) shows the direction bit still active because a second pulse has not yet been detected. The system time out pulse is shown in (v). Since the second pulse has not been detected, an interrupt is triggered which will bring the system back to its steady state.

Figure 4.8: Simulated average energy consumption of speed detector circuit. Notice, the digital circuitry energy consumption is dependent upon the length of the time-out period. As the time-out period increases, the energy consumption also increases. This is because of the rate at which the capacitor takes to fully charge to be considered a logic '1' for the NOR gates in Fig. 4.4

Chapter 5

Improvements and Future Work

Areas of improvement were discussed during analysis and testing of the first version of the vision system. As the reader might have noticed, both the biological vision system and the speed detection circuit require several bias voltages in order to create steady current sources. Floating gate transistors are being considered as an alternative for programming these bias voltages. This could potentially improve the initial design by saving energy

Current research is being conducted on how one would advance the vision system from a one-dimensional vision system, to a two-dimensional vision system. This is proving to be quite a feat, however presented here are some initial considerations and thoughts toward the development of a two-dimensional system.

5.1 Floating Gate Transistors

Floating-gate (FG) transistors have been shown to be very reliable and precise current sources when directly programmed with a combination of hot-electron injection and Fowler-Nordheim tunnelling [28, 29, 30, 31]. Floating-gate MOS transistors are similar to a standard MOS device with one exception. A floating-gate transistor is one which has its gate completely surrounded by SiO_2 . In circuit terms, this means

Figure 5.1: Typical floating-gate transistor configuration.

that the gate has no DC path to ground. A charge can therefore be stored onto the gate of the transistor by coupling it capacitively through an input capacitor C_{in} shown in Fig 5.1. By placing a desired charge on the floating-gate by means of Fowler-Nordheim tunneling or hot-electron injection, the transistor provides a very reliable and precise current source capable of being programmed for any current value.

5.1.1 Floating-Gate Programming

Programming a floating-gate transistor involves setting the DC voltage of the floating-node to a desired DC level by adding or subtracting charge on the floating node [32]. Modifying this charge is done through two different methods known as hot-electron injection and Fowler-Nordheim tunneling [33]. Fowler-Nordheim tunneling is used primarily for removal of charge on the floating node, while hot-electron injection is used for placing charge on the floating node. Hot-electron injection occurs when the electric field in the channel is high enough that it accelerates channel electrons to energies higher than the $Si - SiO_2$ barrier. A detailed analysis of hot-electron injection is explained in [34]. The number of electrons that are injected onto the

gate of the pFET is dependent upon the source-to-drain voltage, the drain current, and the time for which the source-to-drain voltage is maintained higher than the value necessary for injection. Once the charge of each of the floating-gates has been normalized, hot-electron injection will be used to individually program each floating gate to its desired value.

Programming each individual gate involves isolating the floating-gate transistor from the rest of the system first, then applying a sufficient source-to-drain voltage for a specific period of time based on the desired target current of the transistor. A detailed programming scheme is given in [35], [36].

5.1.2 Floating-Gate Transistor Uses

As discussed previously, floating-gate transistors can be used to create a highly accurate current source when used with pFETs. However, there are several other uses for floating-gate transistors besides stable current sources or memory elements in digital logic. One such use is for compensating devices mismatched during the fabrication process. Component mismatch has been addressed through the use of larger devices and layout techniques such as common-centroid layout [32]. Offsets in amplifiers have been addressed using schemes such as auto-zeroing, correlated double sampling, and chopper stabilization [37]. In analog-to-digital converters, it is common to use digital calibration to correct errors due to mismatch [38]. Continuous-time filters employ elaborate tuning schemes to account for variations in transconductance and capacitance [39]. Each of these methods of correction come at the cost of added power consumption, design complexity and chip real estate. By using floating-gate transistors to fix these types of issues, power consumption and design complexity are minimal, and chip real estate is preserved.

5.2 Two-Dimensional Vision System

Several options have for the development of a 2-dimensional vision array are currently being researched. One of these options involve keeping the current system as is, however, two multipliers would need to be added. Therefore, a total of four multiplier would be used at each pixel in order to correlate in not only the +x and -x directions, but also in the +y and -y directions. instead of using two separate multiplier circuits to correlate signals between two adjacent photoreceptors, a total of four multipliers would be used.

The second option involves trying to minimize the number of multiplier circuits used while still gaining the ability to detect 2-dimensional motion. The design can be simplified by studying Fig. 5.2. Instead of having to correlate every pixel, with each adjacent pixel to it, another possibility would develop a system based upon a 3x3 cell as shown in Fig. 5.2. The center pixel would be correlated with each of the surrounding pixels, however, the surrounding pixels will not become correlated with one another. By doing so, 16 multiplier circuits will not be used (2 for each adjacent pair, each representing a direction). Several of these 3x3 arrays would be created in order to design a large scale matrix as shown in Fig. 5.3. However, detecting motion and velocity in this type of system would require much more chip realestate and have a larger impact on power consumption. Also, several capacitors would be needed in order to record analog voltages for interpretation of velocity. This would also mean that several ADC's would be needed in order to read from each of these output voltages. Unfortunately, the mote which was used for these systems discussed here does not posses the capabilities to do this type of analysis. Therefore an alternative needs to be created.

Figure 5.2: New proposed design for two-dimensional motion detection. Here each even row will be correlated with all surrounding photoreceptors, and each odd row will be correlated with the row above and below itself. This will limit the amount of multipliers needed for two-dimensional detection.

Figure 5.3: New proposed design for 2-dimensional motion detection. by taking the 3x3 concept and creating a matrix form of the design several multiplier circuits would not be needed and 2-dimensional motion could still be achieved.

5.3 Next Version of Motion System

The next version of the motion detection wake-up system has been laid out and is awaiting fabrication from MOSIS. The next version of the motion detection wake-up system is composed of the vision detection system and three separate velocity and direction detectors. A total of ten pixels are included in the array, each correlated with its two adjacent neighboring pixels, with the exception of the pixels on the edge of the array. A total of 18 Gilbert multipliers are used so each pixel is correlated with each of its neighbors in order to obtain motion direction in the $+x$ and $-x$ directions. A total of three velocity and direction detection circuits are also used with the 1×10 array vision system. The three separate velocity and direction detection systems each use a pair of pixels, each having different distances separating them, to drive the inputs to the systems comparators. Three systems are used in order to compare system accuracy as well as to test which distance between pixels behaves most accurately. The three separate pairs are as follows; the leftmost pixel with the center pixel, the leftmost pixel with the center pixel, and two pixels adjacent to one another. This new system has been designed using Cadence design software and is being sent to MOSIS for fabrication. The layout for this new system is shown in Fig. 5.4.

Figure 5.4: Next version of the vision wake-up system chip. The chip is composed of a 1×10 array of photoreceptor circuits as well as three separate speed and direction detector circuits. The three velocity detection circuits use three separate pairs of photoreceptor outputs, each pair having different separation distances. Doing so will allow for testing accuracy of the speed detectors as well as finding a distance most suitable for speed detection.

Chapter 6

Conclusion

Presented in this work are three separate systems used for intelligent wake-up of larger scale systems. Chapter 2 presented a system used for spectral analysis wake-up, which was later used in a vehicle detection and classification system. This system was composed of a magnitude detector and several programmable bandpass filters and allowed for tunable quality factors and center frequencies.

In Chapter 3, an analog vision system with programmable speed detection was presented. This system consisted of several photoreceptor circuits developed by Tobi Delbruck, highpass and lowpass filters, and several Gilbert multiplier cells. These separate elements were combined to create a motion detection system. This system was demonstrated to turn on and off a camera network, which in turn saves energy as well as data storage. This system proved to be more energy efficient than a single PIR sensor, which is typically used in home security systems and a Logitech QuickCam S5500.

Chapter 4 demonstrated another alternative to intelligent motion wake-up. With this system, the wake-up could be tuned for object speed and direction. Unlike the systems presented in previous chapters, this system encompassed analog and digital circuitry. This system also utilized less power than a typical PIR sensor and a Logitech QuickCam S5500.

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