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Characterization of Defects on MOCVD Grown Gallium Nitride Using Transient Analysis Techniques

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Characterization of Defects on MOCVD Grown Gallium Nitride Using Transient Analysis Techniques

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**Thesis submitted to the
Benjamin M. Statler College of Engineering and Mineral Resources
at West Virginia University
in partial fulfillment of the requirements for the degree of**

Master of Science

in

Electrical Engineering

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2015

Keywords: Traps, Energy Levels, Capacitance transient, Schottky diode

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ABSTRACT

CHARACTERIZATION OF DEFECTS ON MOCVD GROWN GALLIUM NITRIDE USING TRANSIENT ANALYSIS TECHNIQUES

Sujan Phani Kumar Kasani

Since the invention of the first visible spectrum (red) LED by Holonyak in 1962, there has been a need for more efficient, more reliable and less expensive LEDs. The III-nitrides revolutionized semiconductor technology with their applications in the blue LED's. However the internal quantum efficiency of LED's are limited by the deep level traps in GaN substrate. Traps are defects in the crystal lattice, which depends on growth parameters. These traps act as non-radiative centers where non-radiative recombination occurs without conversion of available energy into light. Characterization of these traps in a material is necessary for better understanding of the material growth quality and resulting device performance. In this work Capacitance-Voltage (C-V) and Deep Level Transient Spectroscopy (DLTS) are conducted which provide electronic properties of trap centers like activation energy, doping concentration and capture cross-section. In n-GaN grown by Metalorganic Chemical Vapor Deposition (MOCVD) on Sapphire two defects types are detected and are characterized by Capacitance-Voltage and Deep Level Transient Spectroscopy. Two deep levels E1 and E2 are typically observed in n-GaN with the activation energies of 0.21eV and 0.53eV at 125°K and 325°K, respectively. The deep level E1 is caused by linear line defects along dislocation cores while deep level E2 is related to point defects. The characterization techniques, experimental systems and preliminary characterization results are discussed in detail.

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Chapter 1: Introduction

1.1 Overview

The field of Semiconductors has revolutionized the world with its devices in everyday life. In recent years III-Nitrides, due to their wide band gaps covering the whole visible region and extending into the UV, has become a driving force for technological advancements. Its applications in many fields attracted attention. Tremendous progress has been made in solid state devices, semiconductor based LEDs and photodiodes. Despite this advancement, the high defect densities in the semiconductor remain an issue. These defects affect the electronic properties of semiconductors and in turn limit the device performance. Defects cause non-radiative recombination, which reduce the intensity of light in LEDs and impact the generation of dark current in photo detectors. Defects also reduce carrier mobility which can impact high frequency operation. Thus knowledge of the mechanisms for carrier recombination is crucial to understanding the performance limits of a particular semiconductor before making it into a device. Hence the electrical properties of traps are of major interest for the design of electronic devices. This work establishes a Capacitance-Voltage (C-V) and Deep Level Transient Spectroscopy (DLTS) setup and presents initial characterization results from the application of these techniques on GaN.

In semiconductor technology, reduction of intrinsic and process induced defects in the crystalline, polycrystalline and amorphous layers is an important goal. Defects arising from impurities, grain boundaries and interfaces result in the creation of traps which capture free electrons and holes. Even at very low concentrations, these trapping centers can dramatically alter device performance [36]. To characterize these defects, a powerful tool is needed. Deep Level Transient Spectroscopy (DLTS) is a well-established technique for the determination of all parameters associated with traps such as density, energy level and thermal cross section. This method is the most sensitive (1 defect in 10^{10} atoms) among the defect characterizing techniques. The DLTS technique requires doping concentration to characterize defects, which is generally provided by C-V profiling and Hall measurements. Application of the method led to the discovery of new phenomena and provided a unique tool for the understanding of materials processing for semiconductor devices [37].

1.2 Effects of traps in p-n junction

A p-n junction is a junction formed between p-type and n-type semiconductor materials of a single crystal of semiconductor [7]. It is the basic unit for several semiconductor devices. Generally, in GaN, the junction is formed by diffusing a p-type layer on n-GaN. Due to the establishment of contact between p-type and n-type layers, electrons diffuse to the p-side and holes diffuse to the n-side which continues until the built in field developed by ionized donors and acceptors in the vicinity of the junction halts diffusion. In a direct semiconductor such as GaN, when an electron recombines with a hole, it is dropped to the lower energy conduction band and the difference in energy is emitted as a photon. This type of recombination is band to band and is called radiative recombination. In this recombination, the energy of the photon is similar to the band gap and is therefore less absorbed so light can escape through the semiconductor.

Figure 1.1: a) Recombination without traps b) Recombination with traps

The wavelength of photon can be calculated by $E = \frac{hc}{\lambda}$

E is the difference between valence and conduction band

h is planks constant; $h = 6.62606 \times 10^{-34} \text{ kg m}^2/\text{s}$

λ is the wavelength of the emitted light

This is not the case when deep level defects are present in a semiconductor. These act like trap centers at intermediate states in the band gap for electrons/holes. These traps prevent band to band recombination of electrons with holes; rather recombination may take place at intermediate levels with random wavelengths reducing intensity of light produced. This type of recombination is called Shockley-Read-Hall recombination [48]. In this type of recombination, both radiative and non-radiative recombination takes place. This does not occur in a perfectly pure semiconductor. Intermediate recombination reduces the internal quantum efficiency of an LED. The presence of deep level impurities is responsible for the current-voltage characteristic collapse seen in III-nitride field effect transistors (FETs) [16-18].

1.3 Defect characterizing techniques

Many characterizing techniques for III-nitride semiconductors have been in use since researchers found defects needing characterization. These techniques started in 1945 with the magnetic resonance method called Electron Spin Resonance (ESR) [10]. ESR is used to find the symmetry, nature and environment of paramagnetic defects. This method has been used for several years to study defects in many semiconductors [11-14]. The sensitivity of ESR is on the order of 10^{12} ions. Optically Detected Magnetic resonance (ODMR) is similar to ESR in studying the nature and symmetry of traps except for the technique used. It is successfully used in II-VI, III-V and amorphous Si [15]. Electrically detected magnetic resonance (EDMR) observed spin dependent electrical properties of the semiconductor, which is mainly used for GaN based devices. Later, positron annihilation spectroscopy is used to detect vacancy defects. Thermalized positrons are trapped in vacant lattice sites, which reduce electron density and increase lifetime. Detection of these quantities gives information like charge state, concentration and defect atomic structure. This technique is especially used to detect vacancy defect states in GaN epitaxial layers. In an effort to characterize different types of traps against a single variable, find information about concentration, energy levels and capture rates of traps, distinguish between majority and minority carrier traps and analyze both radiative and non-radiative centers, a new technique Deep Level Transient Spectroscopy was developed by D.V. Lang [19]

1.3.1 DLTS (Deep Level Transient Spectroscopy): DLTS investigates deep level traps in semiconductor P-N junctions or Schottky barriers' space charge region [20]. Capacitance transients produced by pulsing the Schottky diode junction at different temperatures results in, a spectrum being generated which exhibits a peak for each deep level. The height of the peak is proportional to trap density, its sign allows one to distinguish between minority and majority traps and the position of the peak leads to the determination of fundamental parameters governing thermal emission, activation energy and cross section.

1.3.2 C-V (Capacitance – Voltage): “C-V measurements are well recognized for the valuable information they yield about device and material characteristics” [6]. Capacitance measurement with varying voltage across the p-n or the Schottky diode junction gives the C-V profile. Semiconductor parameters like doping concentration, oxide charges and thickness, threshold voltages and mobile ions can be determined by C-V measurements. Generally C-V is done on Metal-Semiconductor junction, which creates a variable capacitance on applying voltage.

1.3.3 Hall Effect

Magnetic field exerts a transverse force on moving charges, or Lorentz force [39]. When a current carrying material is placed in a magnetic field, the magnetic field exerts force on both charges (semiconductor) in opposite directions. This accumulation of charges develops a voltage difference across a conductive material called the Hall voltage and this effect is called the Hall effect.

Figure 1.2: Hall effect on n-type device [38]

$$V_H = - \frac{IH}{nde}$$

e is the charge of electron

n is density of charge carrier density

I and H are applied current and magnetic field. V_H is Hall voltage.

The Hall-effect measurement is useful to determine the carrier concentration, mobility and resistivity in conducting GaN, and temperature-dependent measurements yield information regarding the thermal activation energies. Even though much progress has been made in doping GaN, there still exist significant challenges, especially with p-type doping. The low hole mobility and low achievable free hole concentration result in large sheet resistance, preventing the fabrication of reliable ohmic contacts with low contact resistivity.

Chapter 2: Literature Review

2.1 Overview: This chapter covers a brief history of Gallium nitride growth, defects, structure, the study of traps and their formation.

The initial attempt to synthesize GaN was made by Juza and Hahn [43]. Later, Ammonia was passed over hot gallium to synthesize the small needles of GaN. Using chemical vapor deposition, Maruska and Titjen succeeded in growing GaN on sapphire substrates in 1969[2]. But there was not much technological advancement due to the p-type doping and poor conductivity restrictions. It then became obvious that doping and defects would play a vital role in the future development of GaN. The early unintentionally doped GaN was believed to be n-type because of the nitrogen vacancies, which are reduced by the AlN buffer layer [23]. The dislocation density for GaN ranges from 10^8 to 10^{12} cm⁻³[24]. The major defects in the GaN epitaxial layer include stacking faults, small angle grain boundaries and nano pipes [25, 27]. Until the 1980s, the importance of carefully optimizing the geometry around defects and the magnitudes of the relaxation energies were not fully realized [40].

The formation of defects depend on many factors, including growth conditions, level of doping, type of impurities, substrate and buffer layer. The GaN grown by Metal-Organic Vapor Phase Epitaxy (MOVPE) on the bulk platelets have a low density of defects [28] with proper cleaning and growth conditions. The AlN/sapphire interface contains a high density of misfit dislocations, which release almost all the misfit between their crystalline lattices at the growth temperature [29]. The lateral overgrowth in III-nitrides is based on the difference in growth rates of GaN in different crystallographic directions.

2.2 Gallium Nitride (GaN)

Gallium nitride is a III-V direct bandgap semiconductor. GaN generally exists in two different crystal structures, as hexagonal Wurtzite and Cubic Zincblende. The former Wurtzite structure is the stable one and the second Zincblende structure is a metastable one. Gallium nitride (GaN) and its ternary and quaternary compounds are prime candidates for fabrication of visible, ultraviolet high-power, high-performance optoelectronic and electronic devices. The physical properties like wide energy band gap and good thermal stability of GaN make it an important semiconductor material for high temperature and high power electronics. High thermal

conductivity compared to silicon and GaAs, makes GaN a better material for heat dissipation in devices.

Figure 2.1: Gallium nitride Wurtzite crystal structure (Wikipedia [47])

Wurtzite GaN	
Bandgap energy	$E_g(200\text{K}) = 3.39\text{eV}$; $E_g(1.6\text{K}) = 3.50\text{eV}$
Temperature coefficient	$dE_g/(dT) = -6.0 \times 10^{-4} \text{ eV/K}$
Pressure coefficient	$dE_g/(dP) = 4.2 \times 10^{-3} \text{ eV/kbar}$
Lattice constant	$a = 3.189\text{\AA}$; $c = 5.185\text{\AA}$
Thermal expansion	$\Delta a/a = 5.59 \times 10^{-6} \text{ K}$; $\Delta c/c = 3.17 \times 10^{-6} \text{ K}$
Thermal conductivity	$k = 1.3 \text{ W/cm K}$
Index of refraction	$n(1 \text{ eV}) = 2.33$; $n(3.38 \text{ eV}) = 2.67$
Dielectric constants	$\epsilon_0 = 8.9$; $\epsilon_\infty = 5.35$
Zincblende GaN	
Bandgap energy	$E_g(330\text{K}) = 3.2 - 3.3 \text{ eV}$
Lattice constant	$a = 4.52\text{\AA}$
Index of refraction	$n(3 \text{ eV}) = 2.9$

Figure 2.2: Properties of GaN (Edgar 1994)

Epitaxy or epitaxial growth is a technique in which a single crystal layer is grown on a substrate. There are many ways to grow GaN. Metal organic Chemical Vapor deposition (MOCVD), Molecular beam epitaxy (MBE) and Liquid Phase Epitaxy (LPE) are generally used. This DLTS characterization is done on GaN grown by Korakakis's group [56] using MOCVD.

2.3 Growth of GaN on MOCVD:

MOCVD is a fast and precise growth technique for many III-N materials. Metal organic chemical vapor deposition (MOCVD) involves a dynamic flow in which gaseous reactants pass over a heated substrate and react chemically to form a semiconductor layer. III-N materials were grown using Trimethylgallium (TMGa), Trimethylaluminum (TMAI), Trimethylindium (TMIn), Silane (SiH₄) and Ammonia (NH₃) as precursors. In (TF-MOCVD) technique, there are two gas flows, main flow and sub flow [1]. The main flow carries reactant gases parallel to the substrate, whereas sub flow gases are inactive and travel perpendicular to the substrate. This sub flow gasses change the direction of the main flow, so that precursors come into contact with the substrate.

Sapphire is used as a substrate with (0001) orientation. Trimethylgallium and Ammonia were used as precursors. N₂ and H₂ gasses are used to carry metal organic precursors to the substrate, which is heated to 1020°C in the stream of H₂, and made to react on the surface to form films. All this process requires a controlled vapor pressure and flow rate of reactants. Many concepts have been developed to accomplish and optimize laminar flow of reactants.

The principal reaction to form GaN is

2.4 Traps

Traps are undesirable defects in the crystal lattice of semiconductor which have different energy levels. Under a non-equilibrium state of a semiconductor, electron-hole pairs are generated. After some time they return to equilibrium by electron-hole pair recombination. If the recombination is between the electron in the conduction band and the hole in valence band then it is called band to band recombination. If one of the carriers (electron or hole) is trapped

between the bands and other carrier is free then this is called recombination on localized states. This capture center of free carrier is called a trap.

Figure 2.3: Transitions in semiconductors a) band to band recombination b) recombination levels c) trapping levels (ASDN.NET educational webportal[49])

L_{R1} , L_{R2} are local recombination levels.

E_{tn} , E_{pn} are trapping levels near conduction and valence band respectively.

N_t , P_t are concentrations of trapping levels near conduction and valence band respectively.

2.4.1 Classification of defects

There are two types of traps, shallow traps and deep level traps. They are distinguished based on the energy levels. Shallow traps exist in the band gap near the bottom of the conduction band or near the top of the valence band. Generally for shallow traps, thermal ionization yields a free carrier and an empty trap. Deep trap is defined by an energy level of trapped carriers whose energy difference between it and the conduction band (for electrons) or valence band (for holes) is much greater than the energy of thermal excitation of the solid at a given temperature.

Impurities, point defects, vacancies, interstitial defects, surface states and interface stresses can act as trapping centers. Dislocation defects, which propagate from the substrate during epitaxy to active region, cause a more rapid degradation of the device, which are not traps. The density of

dislocations in active area can be reduced by small geometry and incorporation of the appropriate buffer layer, which acts as dislocation filters [54].

All these defects which occur in GaN, can be characterized as follows [53]

- a. Point defects, which are also called as zero dimensional defects associated with a single atomic size.
- b. Line defects, which are also called One-dimensional defects associated with a direction.
- c. Planar defects, which are also called Two-dimensional defects associated with a plane or area.
- d. Volume defects, which are also called Three-dimensional defects associated with the volume.

a. Point defects

There are three types of point defects, vacancies, interstitials and substitutional atom defects. If an atom does not occupy a regular crystal site, but occupies a site between regular atoms, it is called an interstitial impurity atom. When an impurity atom substitutes an atom of the host crystal, it is a substitutional impurity. Substitutional impurity is introduced into the crystal either by controlled doping or by contaminants. Oxygen and Carbon are generally the most common contaminants that cause substitutional impurities. Point defects can be characterized as intrinsic and extrinsic point defects. Intrinsic point defects occur due to vacancies, self- interstitial impurities and antisites, as those impurities come from the crystal itself. Extrinsic point defects involve foreign atoms, which occur due to substitutional impurities and interstitial impurities.

b. Line defects

Line defects occur due to the dislocations of atoms. Dislocations occur due to misalignment of atoms or presence of vacancies along a dislocation line in the solid. Dislocations create elastic deformations of the lattice at large distances that cause lattice distortion centered around a line. There are three types of dislocations namely Edge dislocation, Screw dislocation and Mixed dislocation which is both edge and screw dislocations.

c. Planar defects

Planar defects are related to Stacking faults, Stacking mismatch boundaries, Grain boundaries and Twins. Stacking faults are partial displacements, which upset the regular sequence of lattice planes stacking. Stacking mismatch boundaries originate at the substrate or film interface.

Surface steps on a substrate that cause nucleation and growth of separate III-nitrides at different levels create them. Grains of single crystals are present in Polycrystalline materials with different crystallographic orientation. A layer of interconnecting boundary atoms surrounds each grain and it is called a grain boundary. A twin is a defect area, in which a mirror image of the regular lattice is formed. The twin boundary is the mirror plane of the twin formation. The atomic displacements during the twinning increase with the distance from the boundary.

d. Volume defects

The volume defects are related to Inversion domains and Nano pipes. This defect originates from the nucleation layer and has a filamentary nature. Defects due to nanopipes are tunnel like defects that are always aligned along the growth direction of the crystal. The majority of defects are generated at the interfaces with the substrate and the buffer layer. Lattice matching in epitaxial growth is essential between epitaxial layers and the substrate/material on which material is growing. It can be done by choosing substrate/material with a same lattice constant. This can also be done by growing a buffer layer in between material and substrate/material. Here through MOCVD grown GaN, AlN is used as a buffer layer to match the lattice. The structural quality of the GaN layer can be controlled by the growth conditions, especially during the first growth stages.

2.5 Charging and Discharging of Traps in space charge region

Traps charge and discharge with bias. When the bias V_0 is applied to Schottky diode for time t_p the traps fill exponentially with electrons. Traps spill out electrons exponentially under lower bias V_b , which is also referred to as the electron emission from traps. The exponential decay depends on the concentration of filling traps ($n_T, t=0$) and the emission rate (e_n). [51]

$$n_T(t) = n_T(t = 0) e^{-e_n t}$$

The time constant τ of the thermal emission is governed by the thermal emission rate e_n , which depends on the trap energy E_t and on the temperature T

Figure 2.4: Filling and emptying of deep level traps with different bias a) higher bias V_0 b) lower bias V_b ([50])

The emission probability per second e_n is given by

$$e_n = \frac{1}{\tau} = \frac{\sigma v N_c}{g} \exp \frac{-E_T}{kT}$$

Where σ is the trap's capture cross section, v is the average thermal velocity of electrons, N_c is the effective density of states in the conduction band, and E_T is the energy difference between the trap level and the conduction band [52].

Figure 2.5: Band diagram of n-type GaN with trap levels

Table 2.1: Typical Trap properties of MOCVD grown GaN(Hadis Markoc[55])

Trap number	Trap peak temp (T) in °K	Concentration(cm^{-3})	Energy(eV)	Capture cross section(cm^2)
1.	150	2.4×10^{13}	0.246	2.4×10^{-13}
2.	325	6.6×10^{15}	0.536	5×10^{-16}
3.	520	9.6×10^{13}	0.92	1×10^{-15}

The two traps shown in Figure 2.5 are commonly observed in n- GaN. Trap E1 concentrations are lower in n-GaN grown on an n+ GaN substrate, suggesting its correlation with dislocations [56]. The DLTS peak amplitude of trap E1 varies with filling pulse time t_p . This is due to the line defect formed by dislocations. On the other hand, E2 is a dominant peak and the peak increases with increase in Si doping concentration, which induces point defects. This peak can be reduced by doping with In which reduce point defects including native defects.

Chapter 3: DEEP LEVEL TRANSIENT SPECTROSCOPY OF GaN

3.1 Overview

This chapter explains Capacitance-Voltage and Deep Level Transient Spectroscopy techniques. Each technique explanation covers the physics involved and the experimental procedures for acquisition. DLTS measurements are taken after determination of the doping concentration of the semiconductor by C-V measurements.

3.2 Capacitance – Voltage (CV) measurements

C-V is one of the electrical characterizing techniques for semiconductors. It requires either a Schottky diode or p-n junction which forms a space charge region. For this study, p-GaN and n-GaN Schottky diodes are used.

A Schottky diode is a metal semiconductor junction. Before understanding the concept in a metal semiconductor junction let's examine a p-n junction.

Figure 3-1: p-n junction depletion layer with $N_d > N_a$ (Ben G.streetman [36])

Figure 3-2: charge density with in depletion region neglecting free carriers (Ben G.Streetman [36])

When a junction is formed, free carriers diffuse and recombine across the junction to form a depletion layer which is void of free carriers. This region is also called a space charge region. Considering no free carriers in the space charge region, the charge density in the n-type volume within the space charge region is given by q multiplied by the donor concentration N_d and similarly the charge on p side is $-q$ multiplied by the acceptor concentration N_a . Depending on the concentration, the depletion region may vary its distance into p or n type. In the above p-n junction, doping on the n-side is more than the p-side i.e. $N_a < N_d$ so depletion layer extends more into p-side. Generalizing charge density for a junction with a cross sectional area A , charge on either side of the dipole is equal and can be written as

$$q A x_{no} N_d = q A x_{po} N_a \quad 3.1$$

x_{no} is distance encroachment by depletion layer into n-side.

x_{po} is distance encroachment by depletion layer into P-side.

A potential difference develops over the space charge region from n-side to p-side due to the barrier caused by no charge carriers in this region. Using Poisson's equation ($\nabla \cdot E = \frac{\rho_f}{\epsilon}$) the gradient of the electric field is define as

$$\begin{aligned} \frac{dE}{dx} &= \frac{q}{\epsilon} N_d, & 0 < x < x_{no} \\ \frac{dE}{dx} &= \frac{q}{\epsilon} N_a, & -x_{po} < x < 0 \end{aligned}$$

Where, ρ_f is free charge density.

Considering E is zero at the edges of depletion layer, and maximum at center since all electric lines passes thorough $x=0$ plane. Let E_0 be the maximum electric field.

$$\int_{E_0}^0 dE = \frac{q}{\epsilon} N_d \int_0^{x_{no}} dx, \quad 0 < x < x_{no}$$

$$\int_0^{E_0} dE = -\frac{q}{\epsilon} N_d \int_{-x_{po}}^0 dx, \quad -x_{po} < x < 0$$

The maximum value of electric field is $E_0 = -\frac{q}{\epsilon} N_d x_{no} = -\frac{q}{\epsilon} N_a x_{po}$

By using the relation between voltage and electric field, $V_0 = -\int_{-x_{po}}^{x_{no}} E(x) dx$

$$V_0 = -\frac{1}{2} E_0 W = \frac{1}{2} \frac{q}{\epsilon} x_{no} N_d W = -\frac{1}{2} \frac{q}{\epsilon} x_{po} N_a$$

We know $W = x_{po} + x_{no}$ and solving for W using 3-1

$$V_0 = \frac{1}{2} \frac{q}{\epsilon} \frac{N_a N_d}{N_a + N_d} W^2$$

$$W = \left[\frac{2\epsilon}{q} V_0 \left(\frac{1}{N_a} + \frac{1}{N_d} \right) \right]^{1/2} \quad 3.2$$

This shows that the depletion width of a p-n junction is dependent on the contact potential and doping concentrations. Since we are taking C-V measurements on a Schottky diode, the above equation 3.2 is transformed such that it satisfies Schottky diode properties. The major differences between a Schottky barrier and a p-n junction are its typically lower junction voltage, and decreased (almost nonexistent) depletion width in the metal [32]. Since the depletion layer in the metal is so small it can be neglected, and therefore all the depletion and potential difference occur in the semiconductor.

3.2.1 Schottky diodes in n-type GaN

Ni/Au unannealed and Ti/Al/Ti/Au annealed metal contacts are deposited on n-type GaN for Schottky contact and ohmic contact respectively, which forms a Schottky diode. Formation of a Schottky diode on N-type GaN is clearly explained in chapters 4 & 5.

Figure 3-3: a) Metal semiconductor before contact b) Metal semiconductor after contact (Gísli Jóhann Grétarsson[31])

Figure 3-4: Junction formation in metal and n type semiconductor (Ben G.streetman [36])

The electric field and bending of bands within a depletion layer are similar to p-n junction. Here a depletion layer only formed in the semiconductor. Negative charge on the metal is formed because of the positive charge of uncompensated donor ions near the junction. So, W can be calculated by p^+ -n approximation using 3.2. In a p^+ -n junction, neglecting the thin sheet of the

positive layer ($x_{p0} = 0$) and $Na \gg Nd$. This implies $\frac{1}{Na} \ll \frac{1}{Nd}$ and $W = x_{no}$, replacing these quantities in 3.2.

Now,

$$x_{no} = \left[\frac{2\epsilon}{q} V_o \left(\frac{1}{Nd} \right) \right]^{1/2} \quad 3.3$$

3.2.2 Schottky diodes in p-type GaN

Ni/Au annealed and Ti/Al/Ti/Au metal contacts are deposited on P-type GaN for ohmic contact and Schottky contact respectively, which forms a Schottky diode. Formation of a Schottky diode on N-type GaN is clearly explained in chapters 4 & 5.

Figure 3-5: Junction formation in metal and p type semiconductor (Ben G. streetman [36])

When the junction is formed, positive charge is induced on metal due to the negative uncompensated acceptors. Using 3.2,

$$X_{p0} = \left[\frac{2\epsilon}{q} V_o \left(\frac{1}{Na} \right) \right]^{1/2} \quad 3.4$$

3.3 C-V Analysis

A Schottky diode is fabricated on a GaN substrate. In a Schottky diode, metal and semiconductor acts as plates of a capacitor and the depletion region acts as an insulator. This formation gives the capacitance effect which is used to characterize semiconductors by C-V measurements.

Capacitance in the parallel plate capacitor is given by

$$C = \frac{\epsilon_o \epsilon_r A}{d} \quad 3.5$$

d is the depletion layer width (in case of Schottky diode)

ϵ_r is relative permittivity

ϵ_0 is the permittivity of free space

Let's consider n-type first, When a reverse bias voltage V_r is applied to a Schottky diode the built in voltage increases which is equal to $V_0 + V_r$ and here $d = x_{no}$. From 3.3 and 3.5, and substituting these quantities we get

$$N_d = -2 \frac{C^2 V}{q \epsilon_r \epsilon_0 A^2} = -2 \frac{C^3}{q \epsilon_r \epsilon_0 A^2} \left(\frac{dC}{dV_r} \right)^{-1} \quad 3.6$$

Similarly for p-type

$$N_a = -2 \frac{C^2 V}{q \epsilon_r \epsilon_0 A^2} = -2 \frac{C^3}{q \epsilon_r \epsilon_0 A^2} \left(\frac{dC}{dV_r} \right)^{-1} \quad 3.7$$

This is the most useful form, deduced by Hilibrand and Gold. This is used to calculate bulk doping concentration of a semiconductor. By calculating the slope of the graph $\left(\frac{1}{C^2} \right)$ versus V , the doping concentration of the semiconductor is known. V_0 , built in voltage can also be calculated by finding the x-intercept of the graph. [33]

Figure 3-6: C-V measurement graph (Miron J. Cristea[33])

3.4 Deep Level Transient Spectroscopy (DLTS)

DLTS is based on the fact that the capacitance of the space charge region in time depends on the charge state of deep level traps in that region [34]. From 3.6 we can write the capacitance of the junction is

$$C_o = A \sqrt{\frac{\epsilon\epsilon_o q(N_d)}{2V}} \quad 3.8$$

$$V = V_o + V_r$$

Where V_o is the built in voltage and V_r is the reverse bias voltage.

N_d is ionized donor in the space charge region.

Including concentration of traps in the math, let N_t is the trap concentration present in n-sample. Capacitance of the junction now changes due to the extra traps in the depletion region.

$$C_t = A \sqrt{\frac{\epsilon\epsilon_o q(N_d + N_t)}{2(V_o + V_r)}} \quad 3.9$$

Thus the change in capacitance due to recharging these levels is given by

$$\begin{aligned} \Delta C &= A \sqrt{\frac{\epsilon\epsilon_o q(N_d)}{2(V_o + V_r)}} - A \sqrt{\frac{\epsilon\epsilon_o q(N_d + N_t)}{2(V_o + V_r)}} \\ &\equiv C_o \frac{N_t}{2(N_d)} \quad \text{when } N_t \ll N_d \end{aligned} \quad 3.10$$

From 3.10 traps concentration can be calculated

$$N_t = \frac{2\Delta C}{C_o} N_d \quad 3.11$$

Figure 3-7: DLTS experimental procedure [34]

Under reverse bias V_r , pulses with less reverse voltage are applied for certain time t_{imp} . These pulses recharge the charges in the space charge region. Thus the capacitance of junction has a peak and tries to regain its original capacitance C_0 . This is due to the fact that after charging by pulse, the trap concentration decays exponentially with emission probability given by

$$e_{n,p} = \frac{1}{\tau} = \frac{\sigma v_p N_{c;p}}{g} e^{\frac{-E_t}{kT}}$$

σ is trap's capture cross section, $N_{c;p}$ is the effective density of states in the conduction band (for electron emission) valence band(hole emission), and E_T is the energy difference between the trap level and the conduction band[35]. It is very important to find the rate window, which is the time between two points where the difference in capacitance will peak when a trap has an emission rate

$$e_n = \frac{\ln\left(\frac{t_1}{t_2}\right)}{t_1 - t_2} \quad 3.12$$

Figure 3-8: Typical DLTS signal (Leszek Dobaczewski[37])

Thus the exponential dependence of e_n on $1/T$, which is Arrhenius plot, gives E_t . Once after getting E_t and N_d from C-V measurements, one can find the trap density from 3.11 and 3.8.

$$N_t = \frac{2N_d \Delta C (C_r^{-2} - C_p^{-2})^{-1}}{C_r^3 [\exp(-e_n t_1) - \exp(-e_n t_2)]} \quad 3.13$$

C_p and C_r are capacitance at pulse bias and reverse bias respectively.

N_d is doping concentration from C-V

Replacing N_d value from 3.6 in 3.13

$$\text{Trap density } N_t = \frac{4 (V_r - V_p) \Delta C (C_r^{-2} - C_p^{-2})^{-1}}{\epsilon A^2 q C_r^3 [\exp(-e_n t_1) - \exp(-e_n t_2)]}$$

Chapter 4: Metal Contacts on GaN

Metal contacts are essential to form a space charge region for defect characterization using DLTS. p-n junction properties can be achieved by simple metal semiconductor contact. Moreover they are useful when high speed rectification is needed and sometimes metal semiconductor junctions are unavoidable in semiconductors. This chapter deals with Schottky and Ohmic contacts on both n-GaN and p-GaN.

4.1 Schottky Contact

The Schottky barrier is the rectifying barrier for electrical conduction across heterojunction [64]. Schottky contacts are formed between metal and semiconductor materials if there is a large barrier height and also very low doping concentration in the semiconductor material that is less than the density of states in the conduction band or the valence band [58]. The current-voltage characteristics of rectifying metal semiconductor junctions are similar to p-n junction. They differ in current flow and carrier participation. A p-n junction is a bipolar device, whereas Schottky diodes are unipolar devices [62]. The current in Schottky diode is mainly due to the thermionic emission [65], which will be discussed later in this chapter, of carriers over the potential barrier at metal-semiconductor junction [63].

4.1.1 Schottky contact on n-type

When a metal with work function ϕ_m is brought in contact with semiconductor having work function ϕ_s , the semiconductor Fermi level is higher than metal $\phi_m > \phi_s$ so few electrons move from semiconductor to lower energy states in the metal until Fermi levels align at equilibrium. As a result band bending occurs. Then there exists a potential barrier (ϕ_b) which prevents electrons and holes from passing one side to another, which is the difference in work function potentials $\phi_b = (\phi_m - \phi_s)$. Similarly barrier height ϕ_b prevents electron injection from the metal into a semiconductor conduction band which is $\phi_b = (\phi_m - \chi)$

Due to charge neutrality, positively ionized donors in the depletion region of semiconductor are balanced by a sheet of electrons in the metal at the junction. The potential barrier is increased or decreased by applying bias voltage. Schottky contacts, conduct for one bias polarity so they are also called rectifying contacts. The reduction of work function due to the induced positive charge

in metals by negative charges in the semiconductor causes barrier lowering which is referred to as the Schottky effect.

The Energy band diagrams below clearly show the contact characteristics.

Figure 4-1: Energy band diagram of metal and n-type semiconductor ($\phi_m > \phi_s$) a) before contact b) just in contact c) thermal equilibrium (B. Van Zeghbroeck, 2011) [59]

ϕ_b is the barrier height, which is the potential difference between the Fermi energy of the metal and the majority carrier band edge.

ϕ_m is the work function of metal.

ϕ_i is the built in potential which is the difference between the Fermi energy of metal and that of semiconductors.

For an n-type semiconductor the barrier height is given by $\phi_b = \phi_m - \chi$.

Built in potential V_b is the difference between the Fermi energy of the metal and the semiconductor.

$$V_b = \phi_M - \chi - \frac{(E_C - E_{F,n})}{q}, \text{ n-type}$$

Where ' χ ' is electron affinity of semiconductor. Therefore a metal-semiconductor junction forms a barrier when the Fermi energy of metal is somewhere between the conduction and valence band edge. [59]

Figure 4-2: Current Voltage characteristics of Schottky contact on n-type GaN

4.1.2 Schottky contact on p-type

Generally Schottky on p-type is formed when the metal work function is lower than p-type semiconductor work function. At equilibrium, the barrier height prevents the free movement of holes from semiconductor towards metal.

The Energy band diagrams clearly show the contact characteristics and behavior.

Figure 4-3:Energy band diagram of metal and p-type semiconductor a) before b) just in contact c) thermal equilibrium (B. Van Zeghbroeck, 2011)[59]

For *p*-type material, the barrier height is the difference between the valence band edge, and the Fermi energy in the metal is given by $\phi_b = E_g/2 + \chi - \phi_m$, where ' χ ' is electron affinity of semiconductor.

$$V_b = \chi + \frac{(E_C - E_{F,n})}{q} - \phi_M, \text{ p-type}$$

Figure 4-4: Current Voltage characteristics of Schottky contact on p-type GaN

4.1.3 Forward and reverse bias characteristics of Schottky contacts

Forward bias in which a positive lead is connected to the metal and negative lead to semiconductor, the Fermi energy of metal is lowered with respect to the semiconductor. This makes the contact potential reduced from V_b to $V_b - V_a$ by allowing more electrons to diffuse across the depletion layer towards the metal. This gives a larger positive current in forward bias through the junction.

Figure 4-5: Energy band diagram of metal semiconductor in forward bias [67]

When a negative voltage is applied to metal, Fermi energy of the metal is raised compared to semiconductor. Thus, the potential across the junction increases with a large depletion layer. The barrier ϕ_b is independent of applied voltage and restricts the flow of electrons. Thus a negative bias has a no current flow.

Figure 4-6: Energy band diagram of metal semiconductor in reverse bias [67]

The resulting diode current equation is similar to p-n junction's which is

$$I = I_0 \left(e^{\frac{qV}{kT}} - 1 \right)$$

K is Boltzmann constant

T is temperature in kelvin

V is voltage

I_0 is reverse saturation current

Figure 4-7: Typical current-voltage characteristics of Schottky diode (Ben G.streetman[68])

Here I_0 depends on the barrier height and the probability of electron surmounting this is given by the Boltzmann factor.

$$I_0 \propto e^{\frac{-q\phi_b}{kT}}$$

This equation is applicable for a p-type semiconductor as well. Thus a Schottky contact has rectifying behavior in both types of semiconductors. In both cases forward current is due to injection of majority carriers from the semiconductor into metal. Due to the absence of minority carriers, storage delay is prevented which makes a Schottky barrier ideal for high frequency and switching operations.

4.2 Ohmic Contacts

Regardless of the application, voltage and current signals must be brought into, and taken out of the semiconductors through electrical contacts, which must play a critical role of exhibiting a linear relation with respect to applied voltage. These contacts are Ohmic contacts with low contact resistance which does not hinder performance, especially at high frequency and high power where parasitic contact resistance will limit both frequency and power handling [60,61]. There are many requirements in which I-V characteristics should be linear in both biasing conditions and this can be achieved with ohmic contacts. Ohmic contacts are formed when the work function of metal ϕ_m is close to the semiconductors Fermi level ϕ_s .

4.2.1 Ohmic contacts on n-type GaN

The energy band diagram below clearly shows the contact characteristics.

Figure 4-8: Ohmic metal n-type semiconductor contact band diagram a) Before contact b) At equilibrium (Streetman [68])

For n-type material when the work function of the metal is less than the work function of the semiconductor i.e. $\phi_m < \phi_s$, at equilibrium, electrons transfer from metal to semiconductor. This makes the metal Fermi level move downward. Here the barrier to electron flow from metal to semiconductor is small and can be overcome by a small voltage. There is no depletion region in

the semiconductor, because the potential difference required to align Fermi levels at equilibrium calls for accumulation of majority carriers in the semiconductor.

Figure 4-9: Current Voltage characteristics of ohmic contact on n-type GaN

4.2.2 Ohmic contacts on p-type GaN

The energy band diagrams below show the contact characteristics and operation.

Figure 4-10: Ohmic metal and p-type semiconductor contact band diagram a) Before contact b) At equilibrium (Streetman [68])

Similarly for p-type, the work function of the metal is more than semiconductor, $\phi_m > \phi_s$, which makes the hole transfer easy across the junction. Ohmic contact is good when the doping level

near the semiconductor surface is as high as possible. This causes the tunneling with low contact resistance. For p-type, it is difficult to find metals with large enough work function (most metals have less than 5V) to form a good ohmic contact.

Figure 4-8: Current Voltage characteristics of ohmic contact on p-type GaN

Table 4-1: Ohmic metal contact parameters of on GaN.

	metallization scheme	Layer thickness	Condition to form Ohmic contact	Work function(eV)	Specific contact resistivity Ohm.cm ²	Annealed contacts
n-GaN	Ti/Al/Ti/Au	30nm(Ni), 200nm(Au)	ϕ_m close to ϕ_s	$\phi_m = 4.33$ $\phi_s = 4.2-4.3$	$5.43E-5$	Yes
p-GaN	Ni/Au	2nm(Ti),100nm(Al), 30nm(Ti),200nm(Au)	ϕ_m close to ϕ_s	$\phi_m = 5.35$ $\phi_s = 7.3$	$1.34E-2$	Yes

Table 4-2: Schottky metal contact parameters on GaN.

	metallization scheme	Layer thickness	Condition to form Schottky contact	Work function(eV)	Built in potential(eV)	Annealed contacts
n-GaN	Ni/Au	30nm(Ni), 200nm(Au)	$\phi_m > \phi_s$	$\phi_m = 5.35$ $\phi_s = 4.2-4.3$	$V_0 = 1.1$	No
p-GaN	Ti/Al/Ti/Au	2nm(Ti),100nm(Al), 30nm(Ti),200nm(Au)	$\phi_m < \phi_s$	$\phi_m = 4.33$ $\phi_s = 7.3$	$V_0 = 3$	No

4.3 Conduction mechanisms in metal-semiconductor contacts

There are different ways in which conduction takes place in a Schottky contact.

1. Thermionic emission: Thermionic emission is one in which electrons emit over the barrier. It assumes the electron has greater energy than the barrier to overcome it. This happens when the doping level is low, on the order $N_d < 10^{17} \text{ cm}^{-3}$. Due to low doping the chance of tunneling is very much less. [66]

Figure 4-9: Thermionic emission band diagram and I-V curve[66]

2. Thermionic field emission: Thermionic field emission is another type of conduction, in which electrons use thermal energy to tunnel through the thin barrier of upper end of the conduction band. This is more likely when doping level is intermediate $10^{17} \text{ cm}^{-3} < N_d < 10^{18} \text{ cm}^{-3}$.

Figure 4-10: Thermionic-field emission [66]

3. Field emission: Field emission exists when the doping is very high. Here the conduction is almost ohmic-like due to the direct tunneling, which is caused by a narrow depletion layer. The doping concentration is $N_d > 10^{18} \text{ cm}^{-3}$

Figure 4-11: Field emission [66]

From simulation results, Fig.4-15 shows that with increase in the doping concentration, the depletion width of the junction decreases. For $N_d > 10^{18}$, the depletion width is on the order of few hundreds of nm. Here tunneling is easy and the conduction mechanism is field emission.

Figure 4-15: Plot of Depletion width against bias voltage for different doping concentrations.

Chapter 5: Schottky Diode fabrication

Deep Level Transient Spectroscopy (DLTS) measurements require both Ohmic and Schottky contacts. A Schottky diode for DLTS characterization is designed using the Circular Transmission Line Method (CTLM) and fabricated. All the steps, materials and equipment used for this fabrication are explained in this chapter.

5.1 Sample Annealing

Rapid Thermal Annealing (RTA) is a semiconductor process step used for activation of dopants and interfacial reaction of metal contacts. The thermal treatment reduces resistivity by up to six orders of magnitude, thus increasing conductivity [76]. The resistivity of the *p*-GaN was lowest when O_2 was intentionally introduced during activation [77].

For activation of Mg dopants, *p*-GaN is annealed at 800°C in N_2 ambient for 5minutes. During annealing there may be chances of forming a thin oxide layer over the substrate.

Figure 5-12: Side and top view of p-GaN substrate

Figure 5-13: Side and Top view of p-GaN with oxide layer after annealing

RTA is used only for *p*-GaN processing due to its characteristic high resistivity. At room temperature, all dopants in *n*-type GaN are activated so no RTA is required for *n*-type GaN.

5.2 Surface cleaning

The interface between layers of semiconductor with different materials forms the fundamental components. The presence of parasitic resistance and capacitances of interfaces are more pronounced at higher frequencies. Thus, the quality of these interfaces has become an important concern to avoid deteriorating device performance. This makes surface cleaning of samples a fundamentally important step.

Normally surface cleaning is used to degrease, remove surface oxides and remove metal atom contamination [69]. Samples are degreased by dipping in Acetone for 5 minutes. Unfortunately acetone itself leaves residue so this process is followed by dipping the sample in Methanol for 5 minutes and then in deionized water for 5 min. This process is done at room temperature and this will remove organic contaminants present on the surface. The samples are dried with an N₂ blower. The samples are kept in dehydration bake for 30minutes which is preheated to 100°C. It is one of the important steps as contacts may peel off without dehydration bake [70,71].

HCL and HF solutions are known to remove oxides on GaN surfaces [72]. The surface is treated with BOE for 3 minutes, and then cleaned in DI H₂O for 2minutes. It is now treated with diluted HCL (1:1) for 1 minute, followed by cleaning with water for 2 minutes. This process will result in minimum levels of residual O and C. Buffered oxide etch (HF + NH₄OH) bath effectively remove the oxide layer. HF solution is more effective for electrical and chemical passivation of the surface by tying up dangling bonds with atomic hydrogen [73].

Figure 5-14: Oxide layer removal in surface cleaning process

GaN PROCESS FLOW FOR C-V/DLTS CHARACTERISATION

Figure 5-15: Flow chart of Schottky diode fabrication.

Layer1

5.3 Photolithography

Photolithography is the micro fabrication process of transferring geometric shapes on a mask to the surface of semiconductor wafer [74]. The process uses light to transfer patterns from mask to light-sensitive chemical called photoresist followed by a series of chemical treatments, to develop the photoresist pattern exposed to light [75] which finally forms patterns on semiconductor.

There are many steps involved depending on the type of photo resist used: Photoresist application or spinning, soft baking, mask alignment, hard baking, exposure and development.

5.3.1 Spinning: It is a process in which photoresist is uniformly deposited to a specified thickness on surface of substrate. A small quantity of photoresist is usually applied on the center of the wafer and the spun on a spinner which makes the photoresist spread uniformly. The thickness depends on the viscosity of photoresist, spinning speed and time. There are two types of photo resists - positive and negative. For positive resists, the resist is exposed to UV light wherever the underlying material is to be removed. In these resists, exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer [78]. Negative resists behave just in the opposite manner. There are special photoresists which are used in “lift off” techniques which call for a negative wall profile. Even though they are positive resists they are capable of image reversal (IR) resulting in negative patterns on the mask. In this work, a Laurel Technologies 400 spinner is used for spinning image reversal photoresist AZ 5214 for 30 seconds with speed 4000RPM. The thickness obtained for photoresist applied in those conditions is 1.4 μ m.

Figure 5-16: AZ 5214 photoresist coating on GaN substrate

5.3.2 Soft bake: The photo resist coated wafer is prebaked to drive off the excess photoresist solvent on a hot plate at 95°C for 1 minute. This is a critical step as excessive baking destroys photoactive compound and reduces sensitivity. [79]

5.3.3 Mask Alignment and Exposure: It is the next step after soft bake, in which UV light is exposed through a mask on the resist to change the solubility properties. The mask is a square plate with a patterned emulsion of metal film on one side. There are three primary exposure methods - contact, proximity and projection depending on the alignment gap between wafer and mask.

Figure 5-17: Contact, proximity and projection exposure methods (ece,gatech) [74]

For the process used here, the soft baked substrate is placed in proximity exposure in a Suss MA6 Mask Microtech Aligner and UV light (i-line) of intensity $50\text{mJ}/\text{cm}^2$ is illuminated for the time given by

$$t = \frac{50}{\text{sensitivity}} \text{ s}$$

Figure 5-18: a) mask with ring pattern b) side view and top view of GaN during exposure in mask aligner

5.3.4 Hard bake or post exposure bake: In a hard bake, the substrate is baked on a hotplate for 1 minute at 120°C-130°C. Image reversal capability to resist is obtained by a crosslinking agent in the resist which becomes active at temperatures above 110°C for areas which are exposed in mask aligner. After hard bake the exposed areas become insoluble and no longer light sensitive while the unexposed areas still behave like normal photoresist.

Figure 5-19: side and top view of GaN after hard bake

5.3.5 Flood Exposure: A flood exposure of UV light in which no mask is used with intensity 2000 mJ/cm² will now cause all previously unexposed areas of the resist to undergo chemical reaction to make them soluble in developer. OAI UV flood exposure is used to illuminate 365nm UV light. The exposure time is approximately

$$t = \frac{2000}{\text{sensitivity}} \text{s.}$$

Figure 5-20: side and top view of GaN in flood exposure

5.4 Development: In development, the soluble areas of resist get dissolved in developer solution, leaving other areas unaffected. During development, the substrate is treated with AZ MIF 300 developer for 30-45 seconds, and then rinsed in water for 1 minute.

Figure 5-21: side and top view of GaN after development

5.5 Metal Deposition

The widely used technology for depositing metal layers is physical vapor deposition. E-Beam evaporation and sputter deposition are two techniques used in this process. Generally in evaporative deposition, the metal to be deposited is placed in crucible and bombarded with an electron beam in a high vacuum chamber. The beam with high kinetic energy loses energy upon hitting the metal with the release of high thermal energy. Thermal energy heats up the metal causing it to evaporate. With high vapor pressure, the vapor is directed to coat the surface of the wafer.

The metal contact characteristics of GaN are discussed in Chapter 4. In this work, Ni/Au and Ti/Al/Ti/Au contacts are used which have different properties when annealed. After development, the substrate is loaded in a Temescal BJD 2000 E-Beam evaporator. Nickel is allowed to evaporate until 30nm thickness of the layer is deposited. Similarly, gold is allowed to evaporate to 200nm. This forms a Ni (30nm)/Au (200nm) contact which is annealed to form an ohmic contact. All contacts of Ni/Au and Ti/Al/Ti/Au on p and n type GaN are discussed in chapter 4.

Sputtering is another technique used when good step coverage is required. The substrate is placed in a vacuum chamber with the target material and an inert gas is introduced at low pressure. An RF power source causes the gas to become ionized. The ions are accelerated towards the surface of the target, the kinetic energy transfer upon impact causing atoms of the source material to be liberated from the target in vapor form [70] and condense on all surfaces

including the substrate. In this the material is released from the source at a much lower temperature than evaporation.

A Magnetic field can be used to confine electrons near the target surface to greatly increase the possibility of ionizing collisions with the argon gas molecules.

Figure 5-22: side and top view of GaN after metal deposition

5.6 Lift Off

Lift off is an additive technique with photoresist as a sacrificial material. Metal is applied over the patterned photoresist. During this process, the substrate is dipped in acetone for 15 minutes. Photoresist and the metal deposited above it will be removed completely, leaving the metal in a mask pattern shape on the underlying substrate.

Figure 5-23: Side and top view of GaN after lift off

5.7 Contacts Annealing

Rapid thermal annealing is also used for contact annealing to modify its structural properties. AnnealSys AS-Micro Rapid Thermal Annealer has a process chamber made of a quartz tube with water cooled stainless steel flanges. An infrared halogen lamp is used as a heating source [data sheet]. The chamber is coated with reflective coatings to reduce thermal loss and improve uniformity [81]. For contacts annealing the recipe used is 600°C in O₂ ambient for 3 minutes.

Second layer: For the second layer Schottky dot fabrication, all steps are similar to the first layer starting from spinning to lift. For the Schottky dot a new mask shown in fig. 5-13 and Ti/Al/Ti/Au metal composition are used.

Figure 5-24: Mask with dot pattern

Figure 5-25: Schottky contact fabrication process

Third layer: Gold is deposited over contacts as a protective layer. This layer prevents any changes in the properties of the Schottky diode and contacts ripping off when the device is being wire bonded. This is because the wire bonder uses heat and ultrasonic energy to form a bond which may damage the Schottky diode. Generally a 5nm Au layer is sputtered on the contacts using a CVC 610 DC magnetron sputtering station.

Figure 5-26: Au sputtered layer on contacts

Chapter 6: DLTS Setup and DLTS Study of GaN

6.1 Overview

This chapter deals with the instrumentation and setup in DLTS study. Technically, Deep level transient spectroscopy is a C-V measurement over a temperature range. All the hardware equipment used in C-V measurements is used for DLTS along with the temperature variation and controlling equipment. A cryo-refrigerator system is used to bring the temperature down to as low as 15°K in an open loop manner. A temperature controller along with heater wire on the refrigerator sample cold head is used to control the actual temperature of the cold head and sample in the chamber. A pulse generator, capacitance meter and oscilloscope are used to apply bias pulses and to measure capacitance across the Schottky diode respectively to analyze the DLTS-signal.

Figure 6-1: Deep Level Transient Spectroscopy (DLTS) hardware system.

6.2 DLTS Hardware:

6.2.1 Refrigerator system:

The refrigerator used in this work is Model 22 CTI Cryodyne refrigerator, which is a closed cycle helium refrigeration system. It uses helium gas from the helium compressor (cryogenics 8200) to attain low temperatures. High pressure helium gas from a compressor comes through a supply gas line to the regenerator. The regenerator cools the incoming gas and finally the gas exits the cold head through the exit gas line. Using helium adsorbed this system can go down to 10 °Kelvin.

The space around the cold head is evacuated to thermally isolate the cold head from room temperature. No moisture should form on the refrigerator while running, which ensures there is vacuum and no leak in the system. Air is sucked out from the chamber with a vacuum pump. A Leybold trivac vacuum pump is used for this purpose. It is capable of exerting 10^{-3} Torr pressure which can be read on a vacuum gauge attached to the pump.

6.2.2 Temperature Controller

The temperature controller (TC) is used to maintain a particular temperature in the chamber. The TC system has a sensor and heater wire to attain a specified temperature. The DRC 91C is the TC used in this experiment. A sensor is mounted as close as possible to the sample package and the cold head mount to reduce the error in actual temperature and measured temperature. The DT-670C-CU-HT is a silicon diode sensor used for measuring the temperature of the cold head. The temperature range of the silicon diode used is 1.4K to 500K. A heater wire is wound around the cold head. The heater wire used is 32AWG nichrome heater wire, which is capable of handling 50W power supplied from the temperature controller. After selection of set point, the TC attains a particular temperature (Set point) in the chamber by parallel cooling and heating effect. It measures the temperature of the cold head using the sensor and adjusts accordingly the current to a heater or not based on this feedback signal.

6.2.3 Pulse Signal generator

The pulse generator's main purpose is to supply the filling pulse to the Schottky diode. An Agilent 33220A signal generator is used for generating bias pulses in this study. The Agilent 33220A is an arbitrary waveform generator which is free from periodic noise. Pulses with different time period and voltage peaks can be generated. For this study, a pulse with 2Vp-p for 100 μ s is generated in a 1ms waveform.

6.2.4 Capacitance meter

A Boonton 7200 capacitance meter is used for measuring the capacitance of semiconductor devices, which is capable of measuring capacitance in the order of pico Farads. It has a fast response and a recovery time of less than 50 μ s after an overload condition. This capacitance meter is connected across the Schottky diode to measure the capacitance transient. It has both digital and analog capacitance output. Since DLTS measures transient capacitance, an analog capacitance is output from the meter and is displayed on an oscilloscope for measuring change in capacitance over different time windows. This output presents a calibrated, real time reference voltage proportional to the capacitance of the semiconductor under test.

6.2.5 Oscilloscope

An HP 54602B Oscilloscope is used to view the input and output waveforms. Pulse bias input and analog capacitance output display on an oscilloscope. The change in capacitance value is easily measured between rate windows in this oscilloscope using cursors.

6.2.6 Package and connectors:

The GaN sample is mounted on the cold head using a Small Outline Integrated Circuit (SOIC) package. The package is thermally conductive as the sample should be at the same temperature of the cold head. The package is attached firmly to the cold head with silver paste and mechanical clamp setup. The GaN sample is firmly attached to the package with silver paste. Schottky diode contacts are wire bonded to the package.

36AWG Quad twist wires are used as signaling wires through which bias voltage is applied and capacitance values are measured. Twisted pair wires are used to reduce noise due to electromagnetic interference in wires which is cancelled out by comparing signals from both ends.

6.3 Experimental Work

6.3.1 Schottky diode on GaN

Schottky diode has both ohmic and Schottky contacts for DLTS measurements. Electron beam deposited Ni/Au dot contacts, act as Schottky and Ti/Al/Ti/Au rings annealed act as ohmic on n-type. The dots range from 100 to 400 μ m in radius, while the surrounding inner ring radius is 50 μ m greater than the dot radius, to reduce the series resistance as much as possible. The fabrication of the Schottky diode is discussed in chapter 5 in detail.

6.3.2 CV study on GaN

Initially C-V measurements are taken with varying voltage across the Schottky diode and reading capacitance values. From C-V results N_b , the background concentration of the GaN sample is calculated which is explained in section 3.3.

Figure 27-31: Capacitance-Voltage measurement process setup

i. CV analysis on n-GaN:

Shown in Figure 6-32, is a plot of $(1/C^2)$ versus voltage of a n-GaN (1651) sample. The slope of the curve $(1/C^2)$ versus voltage is used in equation 3.7 to determine N_d :

The slope of the curve is calculated using a linear fit between the marked points, which is 1.0275×10^{19} .

Using equation, $N_d = -2 \frac{C^2 V}{q \epsilon_r \epsilon_0 A^2}$, the donor concentration, $N_d = -1.844 \times 10^{17} / \text{cm}^{-3}$.

Figure 6-32: Capacitance-Voltage measurement on n-GaN

ii. **CV analysis on p-GaN:**

Shown in Figure 6-33, is a plot of $(1/C^2)$ versus voltage of a p-GaN (1652) sample. The slope of curve $(1/C^2)$ versus voltage is used in equation 3.7 to determine N_a :

The slope of the curve between the marked points is 1.53×10^{20} .

Using equation, $N_a = 2 \frac{C^2 V}{q \epsilon_r \epsilon_0 A^2}$, the acceptor concentration, $N_a = 1.229 \times 10^{16}/cm^3$.

Figure 6-33: Capacitance-Voltage measurement on p-GaN

6.3.3 DLTS study on GaN

DLTS measurement involves analysis of junction capacitance following a bias pulse over a range of temperature. Initially the vacuum pump valve is opened to pump down the chamber and fully isolate it from the atmosphere. The helium compressor enables the cold head temperature to drop to 15°K. The temperature controller maintains chamber temperature equal to the set point. Set point is increased in intervals of 1°K starting from 25°K to 400°K. At each point of the interval, with pulse generator is in the ON position, the change in capacitance is measured on an oscilloscope. This is done for different rate windows which are selected based on the requirement ($\frac{t_2}{t_1} = K$). The capacitance transients are converted into the DLTS-signal by correlating them. The simplest DLTS correlation is the 2-point correlation, where the capacitance is measured at two times t_1 and t_2 after the end of each filling pulse, and the difference between these two values is displayed:

$$DLTS = a(C(t_2) - C(t_1))$$

The difference is divided with C_0 (capacitance at steady state) to get the normalized values which is discussed in 3.10 and plotted as a function of temperature gives DLTS signal. Rate window

ratio is chosen such that all sweeps should cover the peak signal. Here 1.2 ratio is taken to get 4 windows which cover the entire signal peaks.

The DLTS signal is converted to trap density by using equation 3.11. In this plot two traps are clearly visible around 125°K and at 315°K which is in agreement with the literature [55].

Figure 6-4: DLTS signal of n-GaN with different rate windows. All rate window ratios $R=t_2/t_1$ were made equal to 1.2

Trap Density calculation

The DLTS signal reveals two DLTS peaks which arise from electron emission from two deep levels. DLTS signal at different rate windows we get range of values for peak temperatures

associated with each emission rate and hence each defect. The amplitude of each peak corresponds to a specific trap concentration which can be calculated from equation 3.13

$$N_t = \frac{2Nd\Delta C(Cr^{-2} - Cp^{-2})^{-1}}{Cr^3[\exp(-e_n t_1) - \exp(-e_n t_2)]}$$

C_p and C_r are capacitance at pulse bias and reverse bias respectively.

N_d is doping concentration from C-V

C_p for two peaks is 1100pF and 480pF.

C_r for two peaks is 1133pF and 671pF.

Thus the trap densities of trap 1 and trap 2 are $2.70 \times 10^{14} \text{ cm}^{-3}$ and $3.12 \times 10^{16} \text{ cm}^{-3}$ respectively.

Activation energy and Capture cross-section calculation

Figure 6-5: Arrhenius plot of emission rates against the reciprocal of peak temperatures.

For each measurement the value of $e_n = \ln(\frac{t_2}{t_1}) / \tau$ is calculated for each trap observed. An Arrhenius plot is plotted for values of $\ln(\frac{e_n}{T^2})$ as a function of $1/KT$. The plot can be seen in figure 6-5, where E_a is the slope and $\ln(\gamma \sigma)$ is the y-intercept. It is found that 211meV and 532meV are the observed activation energies of the traps from the Arrhenius plot.

Conclusion and Future Work

The I-V measurement on Schottky diode shows it is almost an ideal diode. Capacitance-Voltage results quantify the doping concentrations of n-GaN and p-GaN which are $1.844 \times 10^{17}/\text{cm}^{-3}$ and $1.229 \times 10^{16}/\text{cm}^{-3}$ respectively. Deep level traps in GaN effect the performance of LED and other devices made out of the GaN. Deep Level Transient Spectroscopy (DLTS) characterizes GaN grown by MOCVD, which reveals two traps in temperature range of 50°K to 400°K. These two traps are commonly observed in n- GaN. The DLTS peak amplitude of trap E1 varies with filling pulse time t_p . This is due to the line defect formed by dislocations. On the other hand, E2 is dominant peak and the peak increases with increase in Si doping concentration, which induces point defects. The traps with thermal activation energies 211meV and 532meV were observed.

However, DLTS for p-GaN is difficult to analyze. The specific contact resistivity of n-GaN ($5.43\text{E-}5 \text{ Ohm.cm}^2$) is less compared to p-GaN ($1.34\text{E-}2 \text{ Ohm.cm}^2$). The limitation in maximum concentration of Mg that can be doped during growth and atoms ionized at room temperature make it difficult to fabricate a tunneling ohmic contact to p-GaN, which caused the DLTS signal distorted.

With cooler growth temperatures surface stress, forming dislocation densities can be reduced which decrease the E1 defect levels. With the decrease in Si concentration during doping, E2 trap densities can be minimized in n-GaN.

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